产品规格书

ASIP-DW1220-5

降压型DC-DC电源SOC模块集
成控制器

FEATURES

- Wide Input Voltage from 2.7V to 16V
  - ✧ 2.7V to 16V with External 3.3V VCC Bias
  - ✧ 4V to 16V with Internal VCC Bias or External 3.3V VCC Bias
- Adjustable Output Voltage from 0.6V to 5.5V
- 5A Continuous Output Current
- 0.5% Reference Voltage across a 0°C to 70°C Junction Temperature Range
- 1% Reference Voltage across a −40°C to 125°C Junction Temperature Range
- Constant On Time (COT) Control
- Stable with low ESR Ceramic Capacitors
- Selectable Switching Frequency from 600kHz, 800kHz and 1MHz
- Selectable Power Save Mode (PSM) for Light Load or Forced Continuous Conduction Mode (FCCM)
- Pre-Biased Start-Up
- Differential Output Voltage Sense
- Output Voltage Discharge
- Output Voltage Tracking and Reference
- Power Good Indicator
- Junction Temperature Range from −40°C to 125°C
- Programable Soft-Start Time
- Programable Current Limit and Cycle-by-Cycle Current Limit Protection
- Hiccup Mode for Short Circuit and Over-Load Protection
- Thermal Shutdown Protection
- Over Voltage Protection
- QFN-29 (7.0mm×7.0mm×3.95mm) Package

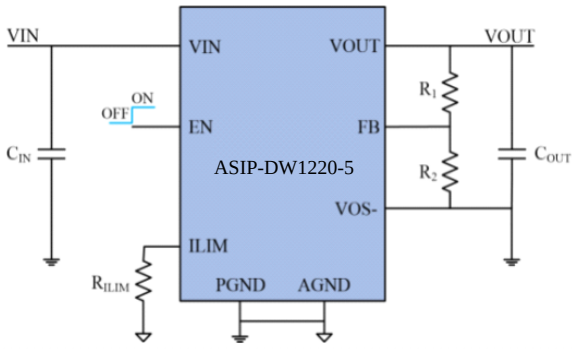
DESCRIPTION

The ASIP-DW1220-5 is a 10A step-down switching mode Power SoC (System on Chip) module with integrated controller, power MOSFET,, inductor and input capacitor in QFN-29 (7.0mm×7.0mm×3.95mm) package. The input voltage is from 2.7V to 16V and the output voltage is adjustable from 0.6V to 5.5V. The ASIP-DW1220-5 also has flexible programable function such a th switchin frequencysoft star time and curren limit. The ASIP-DW1220-5 provides highly efficient output with Constant On Time (COT) control mode for fast transient response and good loop stability. It can work on selectable Power Save Mode (PSM) or Forced Continuous Conduction Mode (FCCM) for light load with excellent load regulation and line regulation. The ASIP-DW1220-5 can also indicate faults and provide overload and short circuit hiccup protection, undervoltage and over voltage protection, and over temperature shutdown protection.

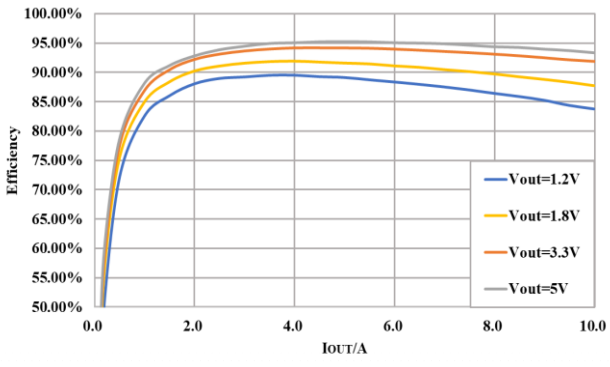
APPLICATIONS

- Telecom
- Servers & Data Centers
- FPGA & ASIC Cards
- Industry Systems

TYPICAL APPLICATION&EFFICIENCY



(Vin=12V, F_{SW}=800kHz, FCCM)

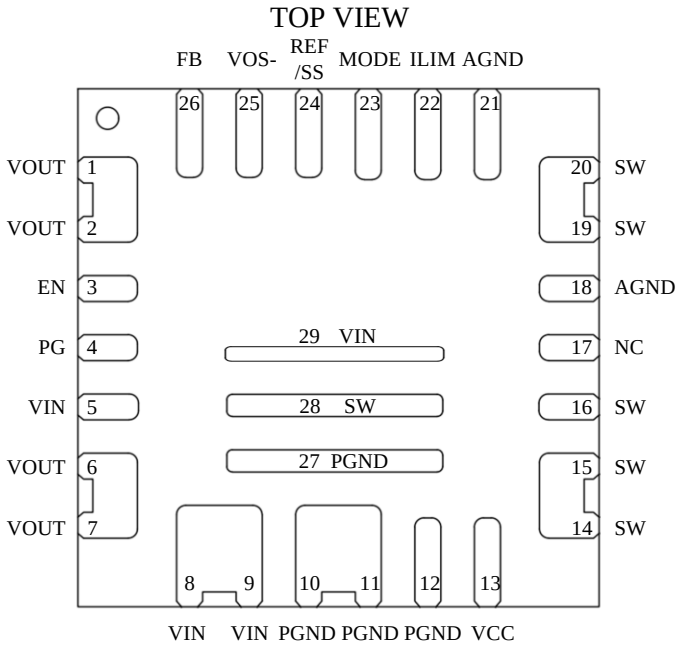


ORDERING INFORMATION

PART NUMBER	TOP MARKING	PACKAGE	MOQ	MSL LEVEL
ASIP-DW1220-5 DQEE	ASIP-DW1220-5 YWWLLL	QFN-29 7.0mm×7.0mm×3.95mm	1000/ Tape & Reel	3

NOTES: Y: Year, WW: Week, LLL: Lot Number.

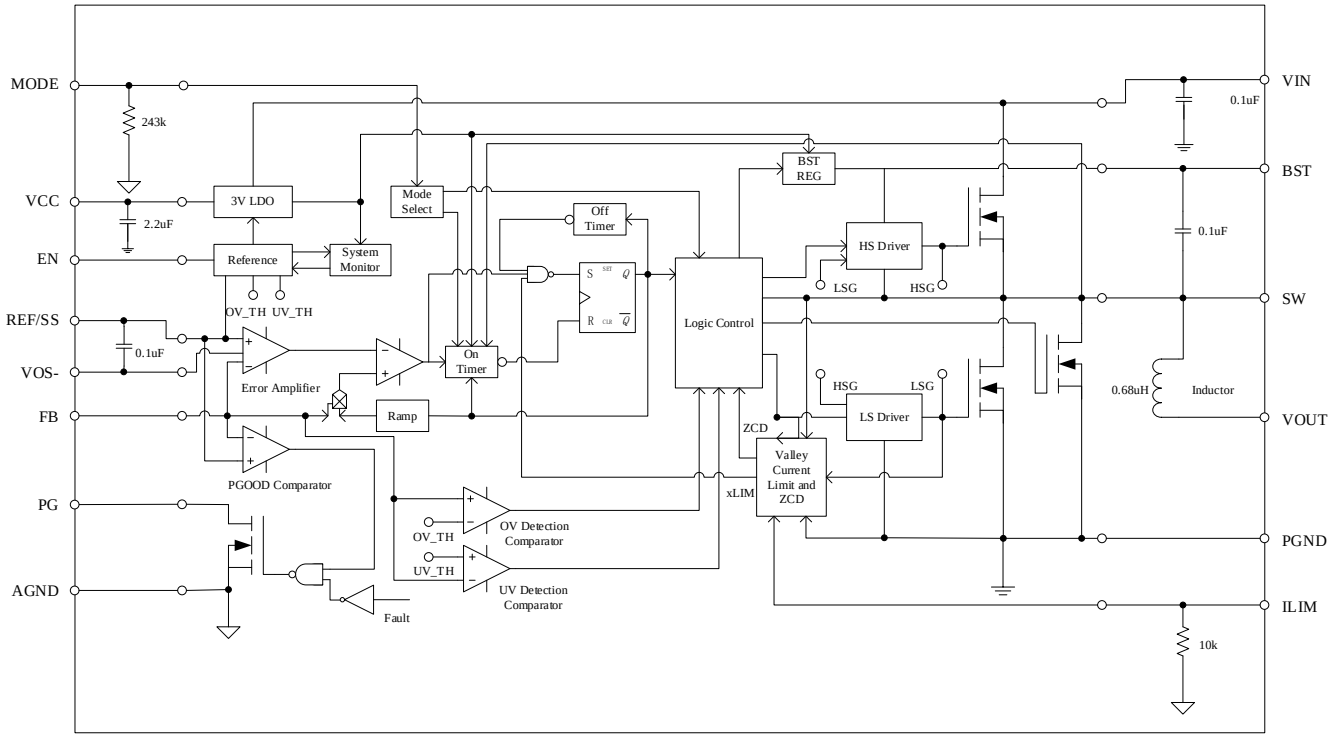
PACKAGE REFERENCE



PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1,2,6,7	VOUT	**Output Voltage Power Rail.** Connect this pin with the load. Output capacitance is recommended to be placed between VOUT and PGND
3	EN	**Enable Control.** Pull this pin low shuts the chip down. Pull it up high enables the chip.
4	PG	**Power Good.** The output of PG is an open drain, a pull-up resistor to power source is needed if used.
5,8,9,29	VIN	**Input Voltage Power Rail.** VIN supplies power to all the internal control circuitry and the power switch. A decoupling capacitor to ground is placed internally.
10,11,12,27	PGND	**Power Ground.**
13	VCC	**Not Connected. Internal 3.3V LDO Output.** An output capacitor to ground have been placed internally.
14,15,16,19,20,28	SW	**Internal SW Pad.** Connect with copper pad for thermal dissipation.
17	NC	**Not Connected. Internal Bootstrap Pad.** A Bootstrap capacitor to SW has been placed internally.
18,21	AGND	**Analog Ground.**
22	ILIM	**Current Limit.** Connect a resister to ground to set the current limit.
23	MODE	**Operation Mode Selection.** Connect a resister to ground to set the operation mode of PSM or FCCM and the switching frequency.
24	REF/SS	**Output Voltage Tracking Reference.** The output voltage tracks this input signal. A decoupling ceramic capacitor recommended to be placed close to this pin. The capacitance determines the soft-start time.
25	VOS-	**VOUT Sense-.** Connect to the negative side of the voltage sense point directly. Connect to PGND to if not used.
26	FB	**Feedback (VOUT Sense+).** Connect this pin with an external resistor divider from the output to VOS- and keep them as close as possible to the pin.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	SYMBOL	MIN	MAX	UNIT
Voltage at Pins	V_{IN}	−0.3	18	V
Voltage at Pins	V_{SW}(DC)	−0.3	V_{IN} + 0.3	V
Voltage at Pins	V_{SW}(25ns)	−5	25	V
Voltage at Pins	VCC/EN		4.5	V
Voltage at Other Pins		−0.3	4.3	V
Junction Temperature Range	T_J	−40	125	℃
Storage Temperature Range	T_S	−65	150	℃
Power Dissipation (T_A=+25℃) Note 1)	P_D Note 1)		4.1	W

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNIT
Input Voltage Range	V_{IN}	4	16	V
Output Voltage Range	V_{OUT}	0.6	5.5	V
Output Current Range	I_{OUT}		10	A
EN Voltage Range	V_{EN}		3.6	V
Junction Temperature Range	T_J	−40	125	℃

THERMAL RESISTANCE

	SYMBOL	MIN	MAX	UNIT
Junction to Ambient	θ_{JA} Note 2)		23	℃/W
Junction to Case	θ_{JC} Note 2)		1	℃/W

NOTES:

1) The maximum allowable continuous power dissipation at any ambient temperature (T_A) is calculated by $P_D(max)=(T_J(max)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the power module will go into thermal shutdown.
2) Measured on EVB, 6-layer PCB 1oZ.

ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_A=25℃, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	with Internal VCC Bias	4		16	V
Input Voltage	V_{IN}	with External VCC Bias	2.5		16	V
Input under Voltage Lockout rising Threshold	V_{UVLO_R}	V_{IN} Rising, V_{CC}=3.3V	2.3	2.4	2.5	V
Input under Voltage Lockout falling Threshold	V_{UVLO_F}	V_{IN} Falling, V_{CC}=3.3V	1.55	1.85	2.15	V
Shutdown Current	I_{SD}	V_{EN}=0V, V_{IN}=5.5V		10	20	μA
Quiescent Current	I_Q	V_{EN}=2V, V_{FB}=0.62V		641	850	μA
EN On Threshold	V_{EN_R}	V_{EN} Rising	1.17	1.22	1.27	V
EN Hysteresis	V_{EN_HYS}			210		mV
Output Discharge FET	R_{ON_DIS}			73	150	Ω
VCC under Voltage Lockout rising Threshold	VCC_{UVLO_R}	V_{CC} Rising	2.65	2.8	2.95	V
VCC under Voltage Lockout falling Threshold	VCC_{UVLO_F}	V_{CC} Falling	2.35	2.5	2.65	V
VCC Regulator	VCC		2.88	3.00	3.12	V
Feedback Voltage	V_{FB_REF}		594	600	606	mV
Current Limit	V_{ILIM}		1.15	1.2	1.25	V
I_{LIM} to I_{OUT} ratio	I_{LIM}/I_{OUT}	I_{OUT} >2A	18	20	22	μA/A
LS Negative Current Limit	I_{LIM_N}			−9		A
Switching Frequency	F_{SW}	MODE=GND, I_{OUT}=0A, V_{OUT}=1V, T_J=-25℃	480	600	720	kHz
		MODE=34.8kΩ, I_{OUT}=0A, V_{OUT}=1V, T_J=25℃	680	800	920	kHz
		MODE=80.6kΩ, I_{OUT}=0A, V_{OUT}=1V, T_J=25℃	850	1000	1150	kHz
Soft-Start Time	T_{SS}	C_{SS} NC		1.5		ms
PG Delay	T_{PG_DELAY}		0.63	0.9	1.17	ms
PG High threshold	$PG_{VTH\_H\_R}$	V_{FB} in respect to V_{FB_REF}	89.5	92.5	95.5	%
	$PG_{VTH\_H\_F}$	V_{FB} in respect to V_{FB_REF}	102	105	108	%
PG Low threshold	$PG_{VTH\_L\_R}$	V_{FB} in respect to V_{FB_REF}	113	116	119	%
	$PG_{VTH\_L\_F}$	V_{FB} in respect to V_{FB_REF}	77	80	83	%

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25℃, unless otherwise noted.

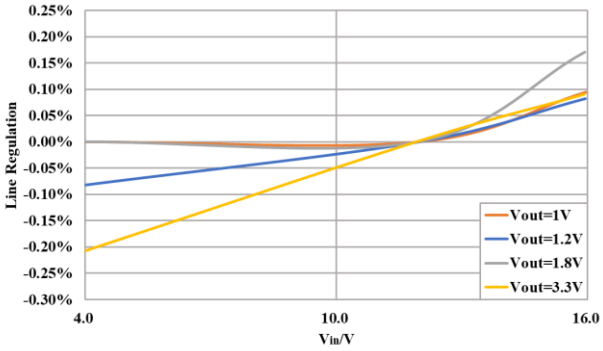
PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Over Voltage Protection	V_{OVP}	V_{FB} in respect to V_{FB_REF}	113	116	119	%
Under Voltage Protection	V_{UVP}	V_{FB} in respect to V_{FB_REF}	77	80	83	%
Thermal Shutdown				160		℃
Thermal Shutdown Hysteresis				30		℃

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, T_A=25℃, F_{SW}=800kHz, V_{OUT}=1.2V, unless otherwise noted.

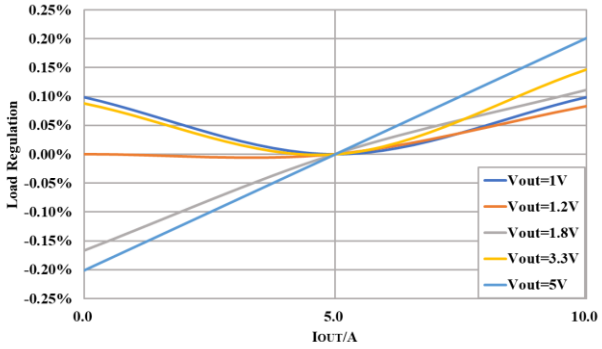
Line Regulation

V_{OUT}=1V/1.2V/1.8V/3.3V, I_{OUT}=10A, V_{IN}=4~16V



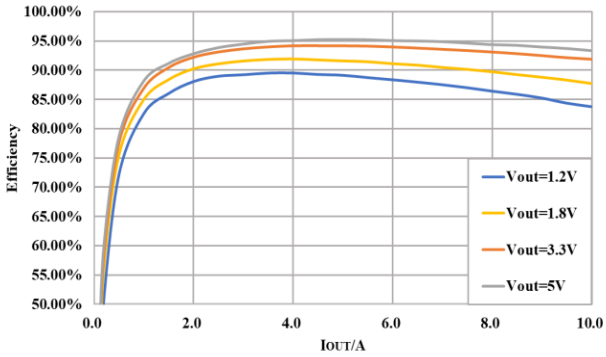
Load Regulation

V_{IN}=12V, V_{OUT}=1V/1.2V/1.8V/3.3V/5V, I_{OUT}=0~10A



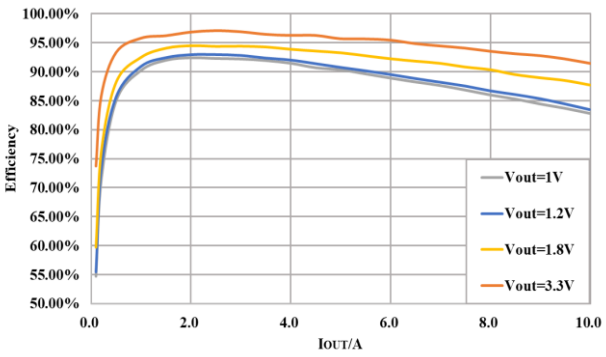
Efficiency

V_{IN}=12V, V_{OUT}=1.2V/1.8V/3.3V/5V, I_{OUT}=0~10A



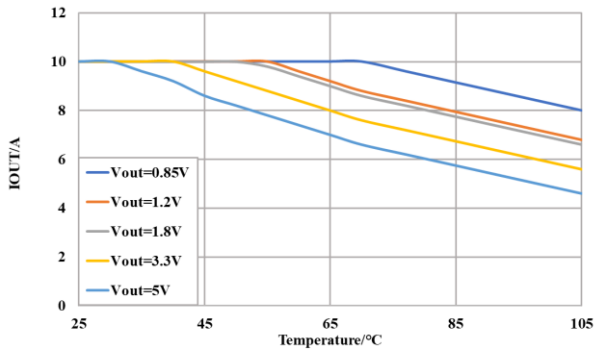
Efficiency

V_{IN}=5V, V_{OUT}=1V/1.2V/1.8V/3.3V, I_{OUT}=0~10A



Thermal Derating

V_{IN} = 12V, V_{OUT}=0.85V/1.2V/1.8V/3.3V/5V

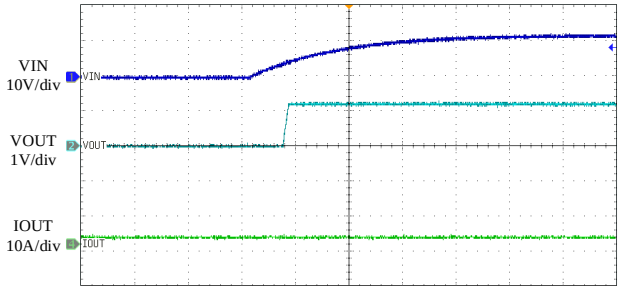


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25℃, F_{SW}=800kHz, V_{OUT}=1.2V, unless otherwise noted.

VIN Start up

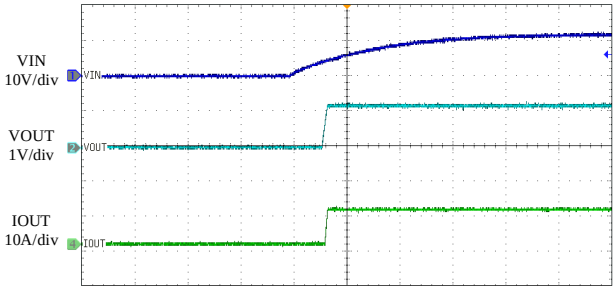
I_{OUT}=0A



20ms/div

VIN Start up

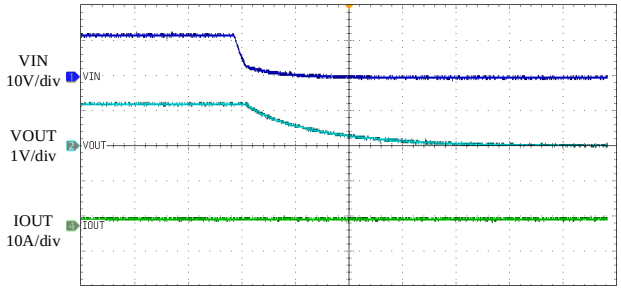
I_{OUT}=10A



20ms/div

VIN Shut down

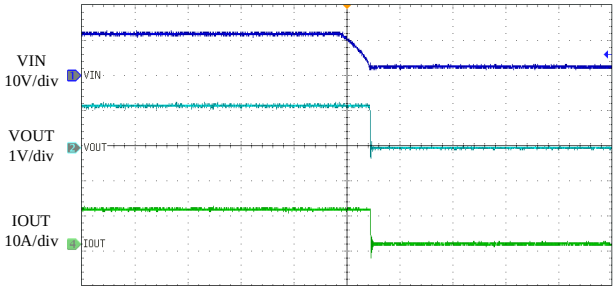
I_{OUT}=0A



400ms/div

VIN Shut down

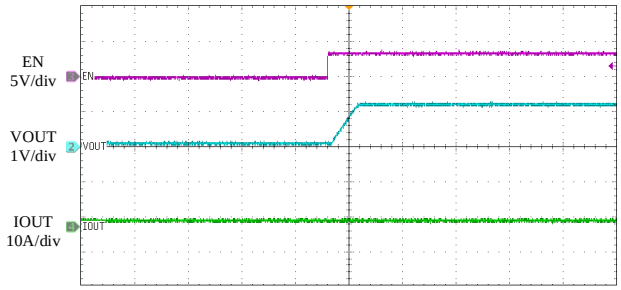
I_{OUT}=10A



2ms/div

EN Start up

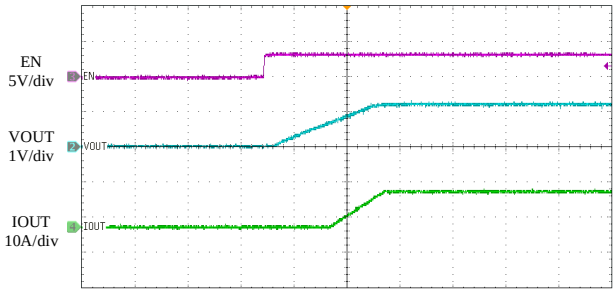
I_{OUT}=0A



4ms/div

EN Start up

I_{OUT}=10A



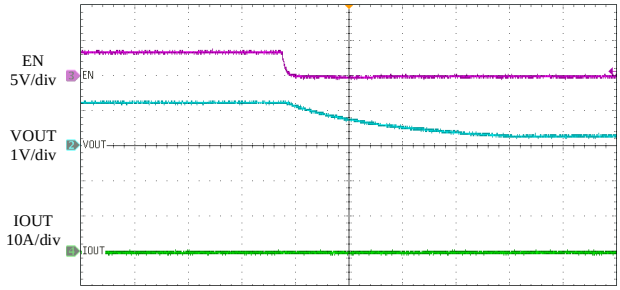
1ms/div

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25℃, F_{SW}=800kHz, V_{OUT}=1.2V, unless otherwise noted.

EN Shut down

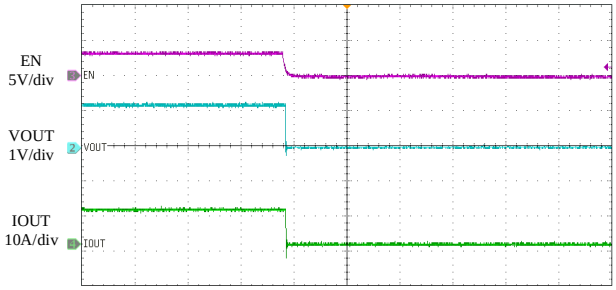
I_{OUT}=0A



4ms/div

EN Shut down

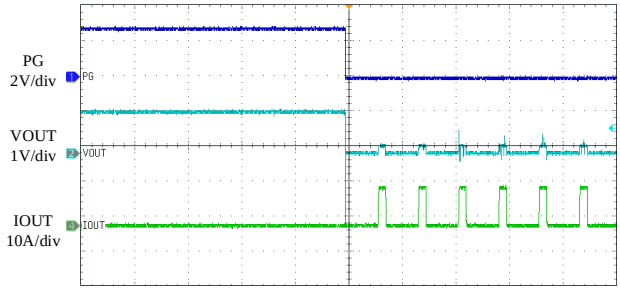
I_{OUT}=10A



4ms/div

SCP Enter

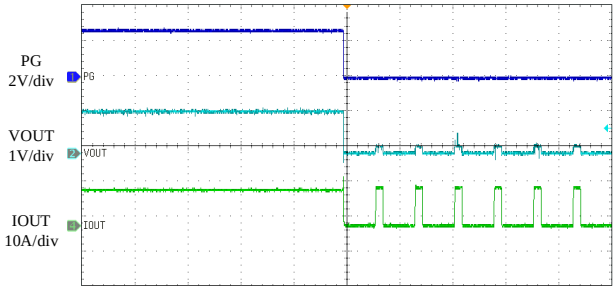
I_{OUT}=0A



20ms/div

SCP Enter

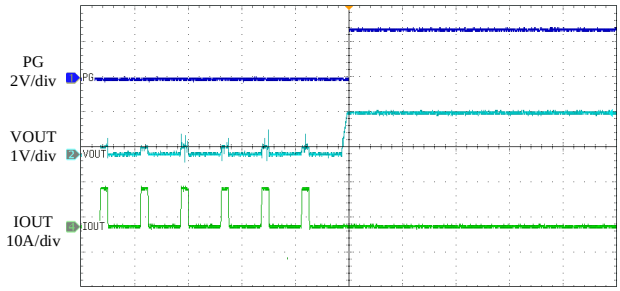
I_{OUT}=10A



20ms/div

SCP Recover

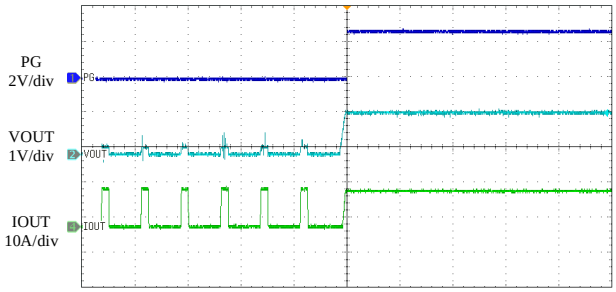
I_{OUT}=0A



20ms/div

SCP Recover

I_{OUT}=10A



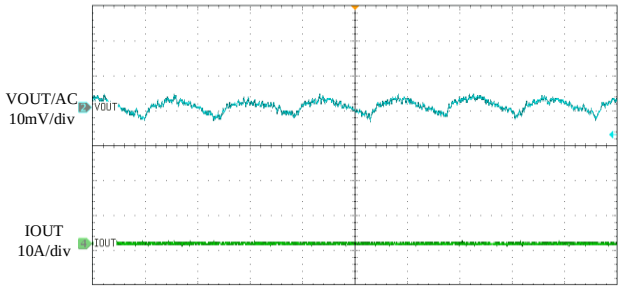
20ms/div

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V, T_A=25°C, F_{SW}=800kHz, V_{OUT}=1.2V, unless otherwise noted.

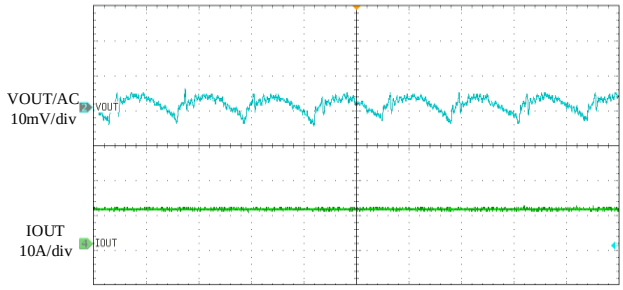
VOUT Ripple

I_{OUT}=0A



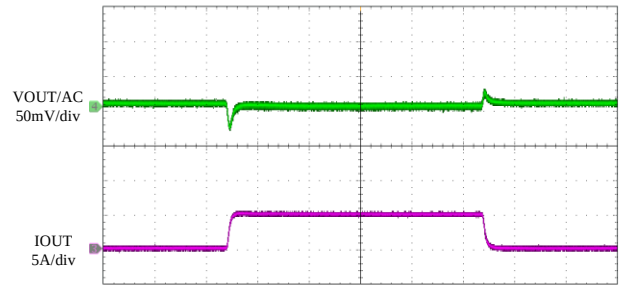
VOUT Ripple

I_{OUT}=10A



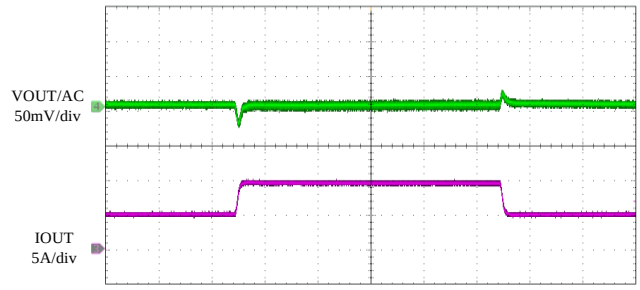
Load Transient

I_{OUT}=0A to 5A, 1A/μs



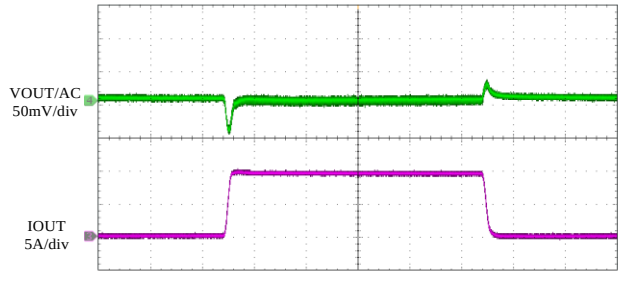
Load Transient

I_{OUT}=5A to 10A, 1A/μs



Load Transient

I_{OUT}=0A to 10A, 1A/μs



OPERATION

The ASIP-DW1220-5 is a 10A synchronous step-down switching mode Power SOC with integrated high-side and low-side power MOSFET, inductor and input capacitor in QFN-29 (7.0mm×7.0mm×395mm) package. And the integrated input coupling capacitor can minimize the parasitic inductance of input circuit and reduce the voltage spike on switching pin which simplify the PCB layout. ASIP-DW1220-5 works on COT control mode that offers excellenttransient response overa wide input voltage range. AUD3683-5can provide excellent load regulation both Pulse Skip Mode and Forced Continuous Conduction Mode for light load, which can be set by MODE. The switching frequency can also be set form 600kHz, 800kHz and 1MHz. Fully integrated protection features include OCP, OVP, UVP and OTP and all this fault can be indicated by PG.The protection function details are shown below. And ASIP-DW1220-5 has a typical 80Ω discharge resister internally which helps the output current drops down quickly when shutdown.

OVER CURRENT PROTECTION (OCP)

ASIP-DW1220-5 has a cycle-by-cycle Low-Side valley current limit protection to prevent inductor current from running away.This current limit value can be programmed as shown in the **USER GUIDE**. When the Low-Side switch reaches the current limit, AUD3683-5 will enter hiccup mode. OCP hiccup mode is active 3ms after ASIP-DW1220-5 is enabled.

If ASIP-DW1220-5 detects an over-current conditio for 31 consecutive cycles, or if V_{FB} drops below the UVP threshold, the device enters hiccup mode. In hiccup mode, the ASIP-DW1220-5 latches off the High-Side MOSFET immediately, and latches off the Low-Side MOSFET after zero-current cross detection (ZCD). The REF/SS capacitor is also discharged. ASIP-DW1220-5 automatically tries to soft start afterabout 11ms. If the over-current condition remains after 3ms of running, the ASIP-DW1220-5. repeats this operation cycle until the over-current condition disappears. ASIP-DW1220-5 also has the low-side negative current limit. When the Low-side MOSFET detects a -9A current, the part turns off the Low-side MOSFET for 200ns to limit the negative current.

OVER VOLTAGE PROTECTION (OVP)

ASIP-DW1220-5 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over voltage condition. If V_{FB} exceeds 116% of V_{FB_REF}, it triggers OVP. When reaching the low-side negative current limit,Low-Side MOSFET turns off for 200ns and the High-Side MOSFET turnson. After200ns, the Low-Side MOSFET turns on again. The ASIP-DW1220-5 repeats this operation to discharge the over-voltage on the output. And ASIP-DW1220-5 exits OVP mode when V_{FB} drops 105% of the regulation.However, ASIP-DW1220-5 employs output sinking mode (OSM) to regulate the output voltage to the target when V_{FB} exceeds 104% of V_{FB_RE} but is below the OVP threshold. During OSM , the Low-Side MOSFET remains on until it reaches the -5.5A negative current limit. Upon reaching -5.5A, the Low-Side MOSFET turns off for 200ns and the HighSide MOSFET turns on during this period.After 200ns, the Low-Side MOSFET turns on. The ASIP-DW1220-5 maintains this operation until V_{FB} drops below 102% of V_{FB_REF}. Once it does, the ASIP-DW1220-5 exits OSM after 15 consecutive cycles of FCCM.

OVER TEMPERATURE PROTECTION (OTP)

ASIP-DW1220-5 will stop switching when the junction temperature exceeds typically 160 °C.The device will power up again when the junction temperature drops below typically 130°C.

USER GUIDE

Setting the Output Voltage

The output voltage is set by the external feedback resistor divider as the typical application circuit on Page 1. The top feedback resistor R_1 can impact the loop stability, so its recommended value is 2kΩ. The bottom feedback resistor R_2 can be calculated as:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{FB}} - 1}$$

Table 1 lists the recommended feedback resistor values for common output voltages when R_1 is 2kΩ.

Table 1：FB Resistor Value for Common Output Voltages.

V_{OUT}	R_2
5V	272Ω
3.3V	442Ω
1.8V	1kΩ
1.2V	2kΩ
1.0V	3kΩ

And a feedforward capacitor C_{FF} is recommended for better load transient response, which typical value is 4.7nF.

Input Capacitor Selection

The input current of the step-down converter is discontinuous with sharp edges, therefore an input filter capacitor is necessary. For better performance, low ESR ceramic capacitor with X5R or X7R dielectrics are highly recommended because of their lowest temperature variations. The RMS current of the input capacitor is calculated:

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)}$$

in which D is the Duty Cycle and when the current is continuous, $D=V_{OUT}/V_{IN}$; I_{OUT} is the output load current. As the equation above, when D is 0.5, the highest RMS current is approximately:

$$I_{CIN\_RMS} = \frac{I_{OUT}}{2}$$

So, it is recommended to choose the capacitor with the RMS current rating higher than 1/2 I_{OUT}.

The power dissipation on the input capacitor can be estimated with the RMS current and the ESR resistor. Electrolytic or tantalum capacitors can also be used as there has been a small size 0.1μF ceramic capacitor placed closed to VIN and GND in ASIPDW1220 -5 already.The input voltage ripple caused by the capacitor can be calculated as:

$$\Delta V_{CIN} = \frac{I_{OUT}}{F_{SW} \cdot C_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

in which, F_{SW} is switching frequency.

Output Capacitor Selection

An output capacitor is required to keep stable output voltage. To minimize the output voltage ripple, low ESR ceramic capacitors should be used. The output voltage ripple can be estimate as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \cdot F_{SW}^{\ 2} \cdot C_{OUT} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In which, L is the inductor, which value is fixed at 0.68μH internally. If electrolytic or tantalum capacitor are used, the ESR will dominate the output voltage ripple as:

$$\Delta V_{OUT} = R_{ESR} \cdot \frac{V_{OUT}}{F_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Enable Control

When input voltage is above the under-voltage-lock-out threshold, ASIP-DW1220-5 can be enabled by pulling the EN pin.

- EN can be driven by a logic signal to enable ASIP-DW1220-5. ASIP-DW1220-5 can be enabled
- by pulling the EN pin to above 1.22V. EN pin can be connected to VIN directly by a pull-up resister R_{PULL_UP}. As the maximum current going in to EN should be keep under 50μA, the R_{PULL_UP} can be calculated as:

$$R_{PULL\_UP}(k\Omega) \geq \frac{V_{IN}(MAX)}{0.05(mA)}$$

- The UVLO of the input voltage also can be programmed by a resister divider connected between EN and AGND. The pull up resister R_{UP} and the pull-down resister R_{DOWN} can be calculated as:

$$V_{IN\_UVLO} = V_{EN\_R} \cdot \frac{R_{UP} + R_{DOWN}}{R_{DOWN}}$$

The voltage of EN should not exceed 3.6V when choosing these resisters and the typical value of V_{EN_R} is 1.22V.

Setting Power Good Indictor

ASIP-DW1220-5 has an open drain PG indicator. pull-A up resistor to VCC or any other power source less than 3.6V is needed if used and its recommended value is about 10kΩ. PG will be pulled dow when the output voltage is out of regulation, otherwise PG is pul led up.PG goes high after a 0.9ms delay when V_{FB} reach es 92% of the regulation. The PG is latched low when V_{FB} drops to 80% or exceeds 116% of the regulation a nd will be pulled high after a new soft start.

Mode Selection & Setting Switching Frequency

ASIP-DW1220-5 can work on FCCM or PSM under the light load by selecting different resister connected with MODE pin. And the switching frequency is also set by this pin. Table 2 shows the value of the resister for different operating mode and switching frequency.

Mode	Light-Load Mode	F_{SW}
VCC	PSM	600kHz
Float (Default)	PSM	800kHz
243kΩ (±20%) to GND	PSM	1000kHz
GND	FCCM	600kHz
34.8kΩ (±20%) to GND	FCCM	800kHz
80.6kΩ (±20%) to GND	FCCM	1000kHz

Setting Current limit

ASIP-DW1220-5 features a current sens and a configurable current limit threshold. By using a resistor (R_{ILIM}) from ILIM to GND, the current limit is set as:

$$\frac{R_{ILIM}(M\Omega) \times 0.01}{R_{ILIM}(M\Omega) + 0.01} = \frac{V_{ILIM}}{G_{CS} \cdot (I_{ILIM} - \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \cdot \frac{1}{2F_{SW}(MHz) \cdot L(\mu H)})}$$

in which, V_{ILIM} =1.2V, G_{CS} =20μA/A, L=0.68μH.

Table 3 shows the recommended value of the resister R_{ILIM} for different operating mode.

Table 3: R_{ILIM} & Operation

Operation	F_{SW}(Default)	I_{LIM}	R_{ILIM}
V_{IN}=12V, V_{OUT}=5V	800kHz	10A	40kΩ
V_{IN}=12V, V_{OUT}=3.3V	800kHz	10A	30kΩ
V_{IN}=12V, V_{OUT}=1.8V	800kHz	10A	22kΩ
V_{IN}=12V, V_{OUT}=1.2V	800kHz	10A	20kΩ
V_{IN}=12V, V_{OUT}=1V	800kHz	10A	18kΩ

Setting Output Voltage Tracking Reference

ASIP-DW1220-5 provides an analog input pin REF/SS to track another power supply or accept an external reference. When an external voltage signal is connected to REF/SS, it acts as a reference for the ASIP-DW1220-5 output voltage. V_{FB} follows this external voltage signal and the soft-start settings are ignored. The REF/SS input signal ranges from 0.3V to 1.4V. During initial start-up, REF/SS must reach 600mV to ensure proper operation. After that, it can be set to any value between 0.3V and 1.4V.

Setting Soft Start Time

ASIP-DW1220-5 has 1.6ms default soft-start timer internally. The time can be increased by adding an external capacitor C_{SS} between REF/SS and GND. C_{SS} can be calculated as:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \cdot 36(\mu A)}{0.6(V)} - 100(nF)$$

Pre-Biased Start-Up

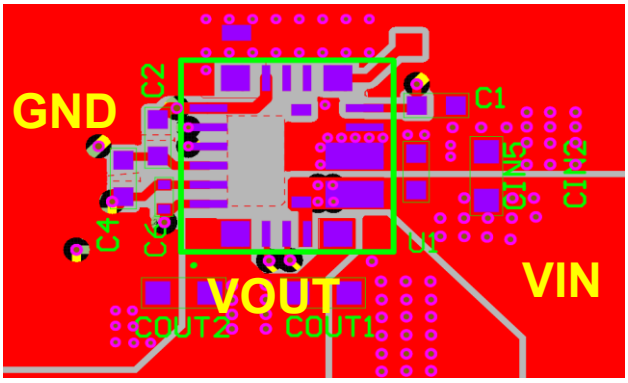
The ASIP-DW1220-5 has been designed for a start-up in to pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the High-Side and Low-Side MOSFETs until the voltage on the REF/SS capacitor exceeds the sensed output voltage at FB. If the internal BST voltage (from BST to SW) is below 2.3V before the REF/SS voltage reaches the pre-biased FB level, the Low-Side MOSFET turns on to allow the BST voltage to be charged through VCC. The Low-Side MOSFET turns on for narrow pulses, so the drop in the pre-biased level is negligible.

PCB Layout Guide

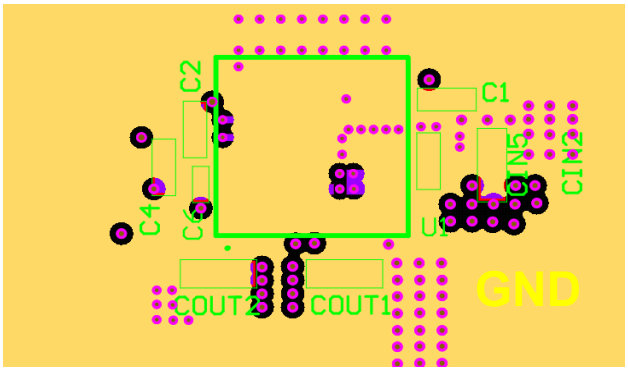
To optimize the electrical and thermal performance, some PCB layout guidelines should be considered as below:

1. Use wide trace for the high current paths and keep it as short as possible. It helps to minimize the PCB conduction loss and thermal stress.
2. The ASIP-DW1220-5 has integrated the inputcoupling capacitor, and it is also better to place other input capacitors close to VIN and GND.
3. Connect all feedback network to FB shortly and directly and keep it as close to the chip as possible.
4. Keep the components away from the SW to prevent stray capacitive noise pick-up.
5. The GND should be connected to a strong ground plane for better heat dissipation and noise protection. And place as many PGND vias as possible.
6. ASIP-DW1220-5 support remote voltage sense for output voltage to compensate for any voltage drop in the leadstraces with heavy loadcurrent by regulating the output voltage at the output terminals of the supply. Make Sure that differentiallines are used to do Output Voltage Sensefrom capacitor terminals.

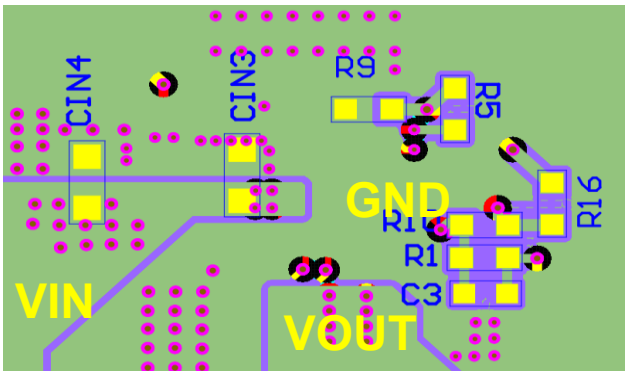
Figure 1 gives a good example of the recommended layout.



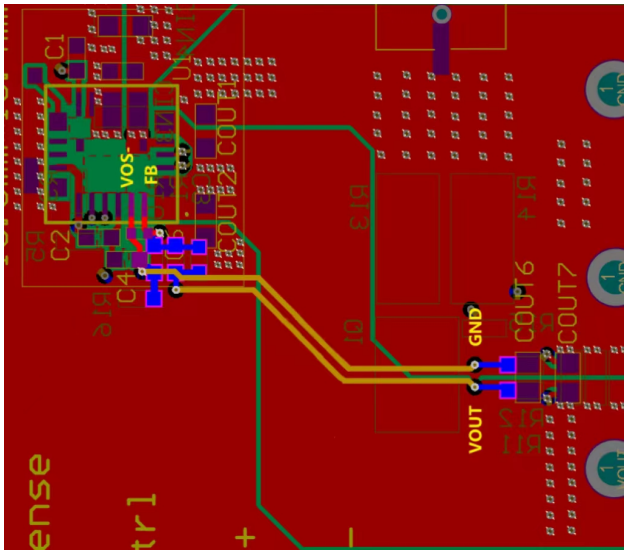
（a） Top Layer



（b）Inner Layer 1/2/3/4



（c）Bottom Layer



（d）Remote Sense Traces

Figure 1. Recommended Layout

TYPICAL APPLICATION

- **VIN=12V**

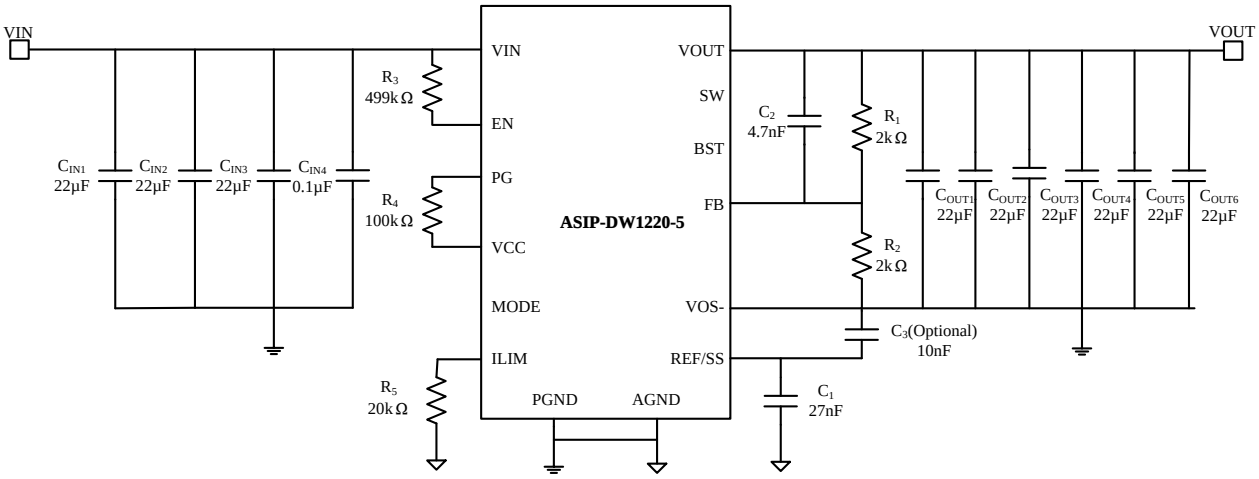


Figure 2. Typical Application Circuits of ASIP-DW1220-5 for 12V Input 1.2V@10A Output, Fsw=800kHz

Table 4：Reference Design for 12V Input

VOUT	CIN	COUT	VOUT Ripple	R_1	R_2	R_5	I_{LIM} (Fsw=800kHz)
5.0V	100uF（E-CAP）+2×22uF	9×22uF	35mV	2kΩ	272Ω	40kΩ	10A
3.3V	5×22uF	8×22uF	25mV		442Ω	30kΩ	10A
1.8V	4×22uF	7×22uF	18mV		1kΩ	22kΩ	10A
1.2V	3×22uF	6×22uF	12mV		2kΩ	20kΩ	10A
1.0V	2×22uF	6×22uF	10mV		3kΩ	18kΩ	10A

NOTES:

CIN is the sum of the input capacitors, COUT is the sum of the output capacitors, please refer to Figure 2 for parameters of other components.

- **VIN=5V**

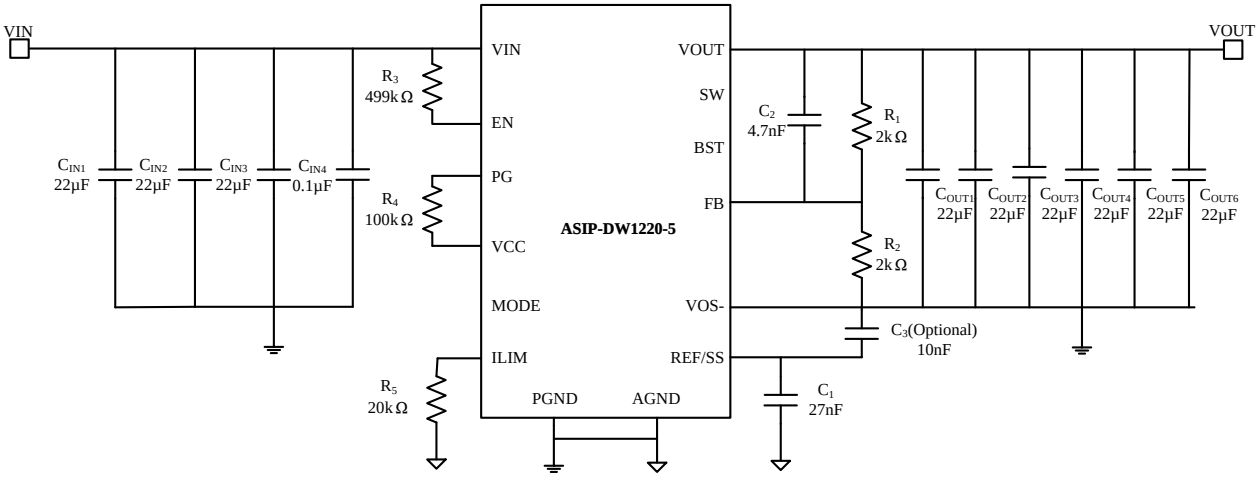


Figure 3. Typical Application Circuits of ASIP-DW1220-5 for 5V Input 1.2V@10A Output, Fsw=800kHz

Table 5：Reference Design for 5V Input

VOUT	CIN	COUT	VOUT Ripple	R_1	R_2	R_5	I_{LIM} (Fsw=800kHz)
3.3V	5×22uF	8×22uF	25mV	2kΩ	442Ω	30kΩ	10A
1.8V	4×22uF	7×22uF	18mV		1kΩ	22kΩ	10A
1.2V	3×22uF	6×22uF	12mV		2kΩ	20kΩ	10A
1.0V	3×22uF	6×22uF	10mV		3kΩ	18kΩ	10A

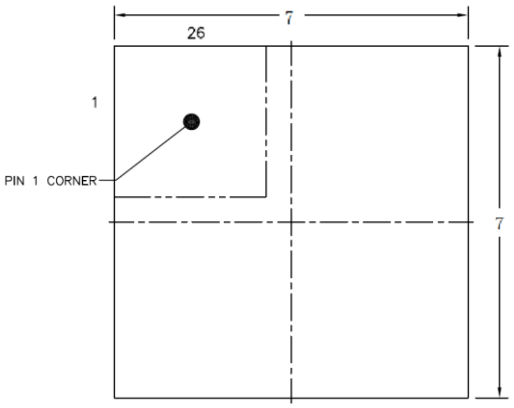
NOTES:

CIN is the sum of the input capacitors, COUT is the sum of the output capacitors, please refer to Figure 3 for parameters of other components.

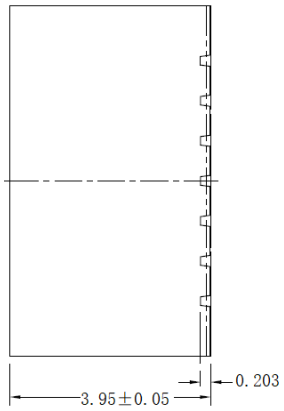
PACKAGE INFORMATION

QFN-29 (7.0mm×7.0mm×3.95mm) Package

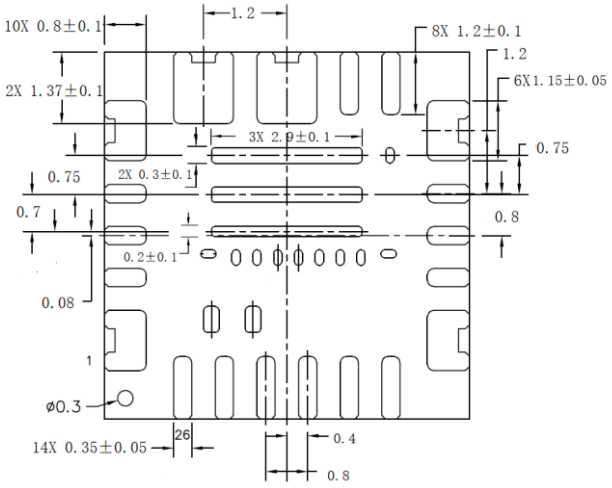
TOP VIEW



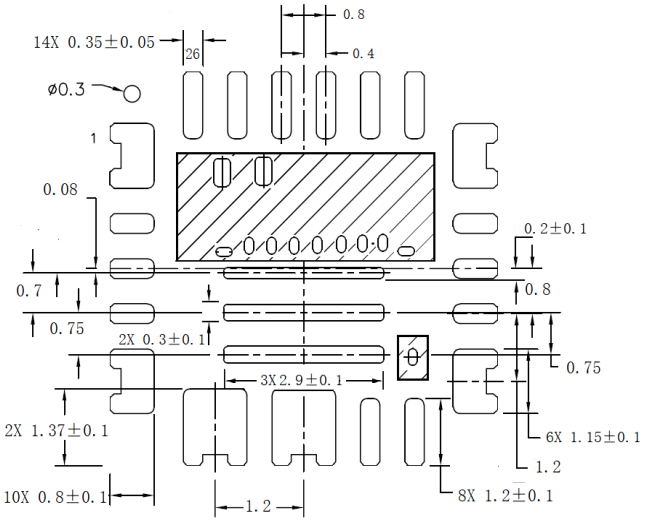
SIDE VIEW



BOTTOM VIEW



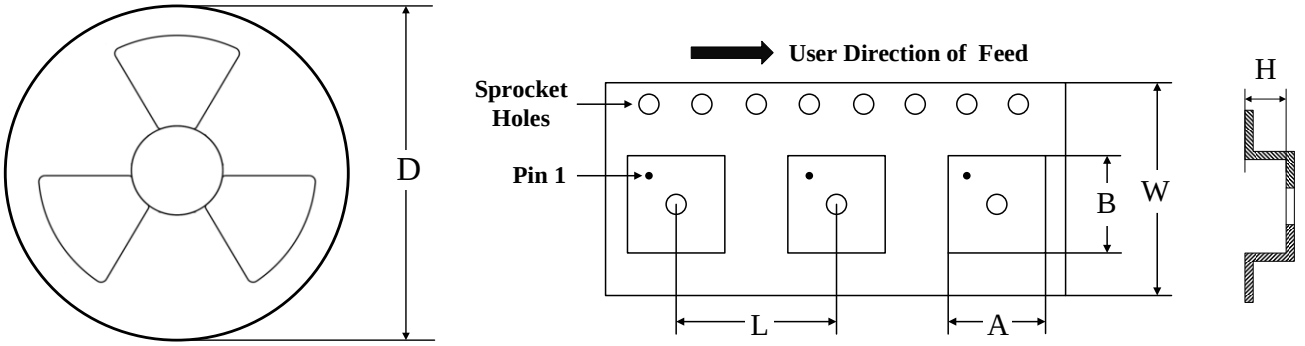
RECOMMENDED LAND PATTERN



NOTES:

1) **All dimensions are in MM.**
2) **The shaded area is the keep-out zone. Not to connect to any electrical or mechanical area.**

CARRIER INFORMATION



Part Number	Package	Quantity /Reel	D	A	B	L	W	H
ASIP-DW1220-5 DQEE	QFN-29 (7.0mm×7.0mm×3.95mm)	1000	13 in	7.7mm	7.7mm	12mm	16mm	4.2mm