

Feature

- Split Gate Trench Technology
- Low RDS(ON)
- Low Gate Charge
- Low Gate Resistance
- 100% UIS Tested

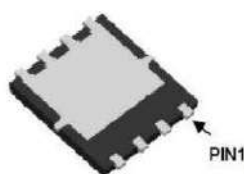
Product Summary



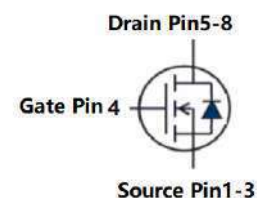
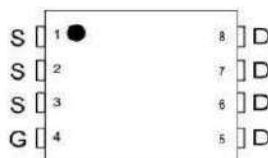
V_{DS}	40	V
$R_{DS(on), Typ @ V_{GS}=10 V}$	3.3	mΩ
I_D	75	A

Application

- Power Switching Application



DFN5*6-8



N-Channel

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

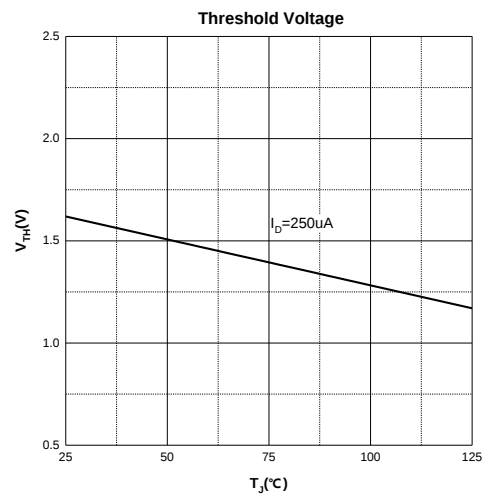
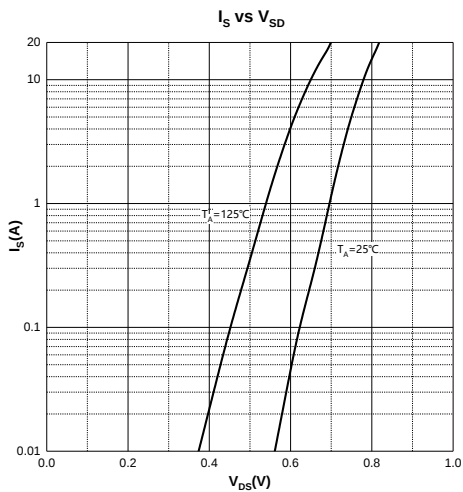
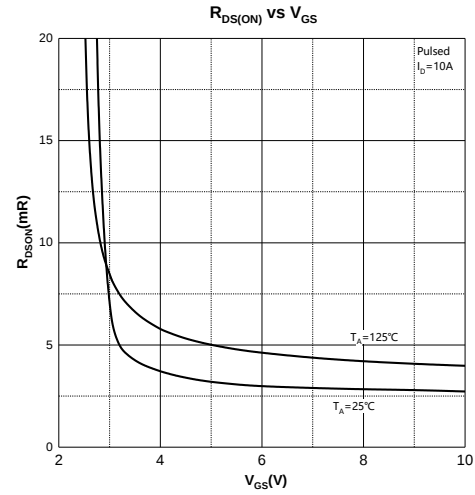
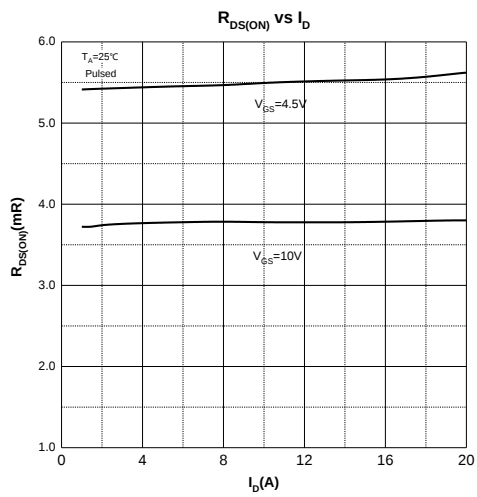
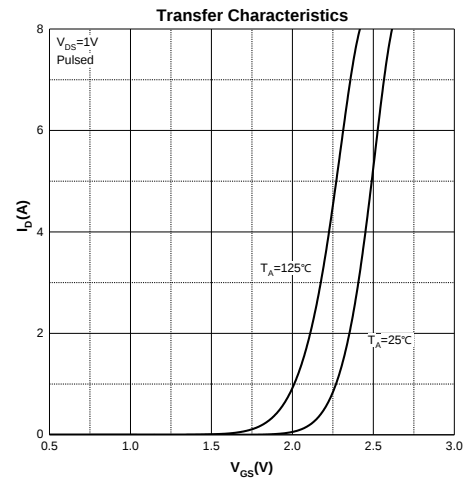
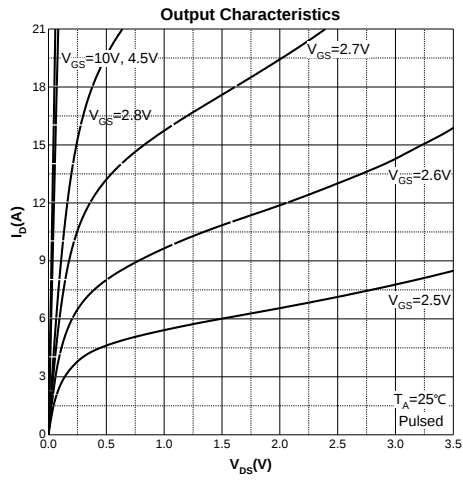
Parameter		Symbol	Value	Unit
Drain - Source Voltage		V_{DS}	40	V
Gate - Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^\circ\text{C}$	I_D	75	A
Continuous Drain Current ¹	$T_C = 100^\circ\text{C}$	I_D	67	A
Pulsed Drain Current ²		I_{DM}	300	A
Single Pulsed Avalanche Current ³		I_{AS}	31	A
Single Pulsed Avalanche Energy ³		E_{AS}	240	mJ
Power Dissipation ⁵	$T_C = 25^\circ\text{C}$	P_D	83	W
Thermal Resistance from Junction to Ambient ⁶		$R_{\theta JA}$	62	$^\circ\text{C/W}$
Thermal Resistance from Junction to Case		$R_{\theta JC}$	2.4	$^\circ\text{C/W}$
Junction Temperature		T_J	150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55~ +150	$^\circ\text{C}$

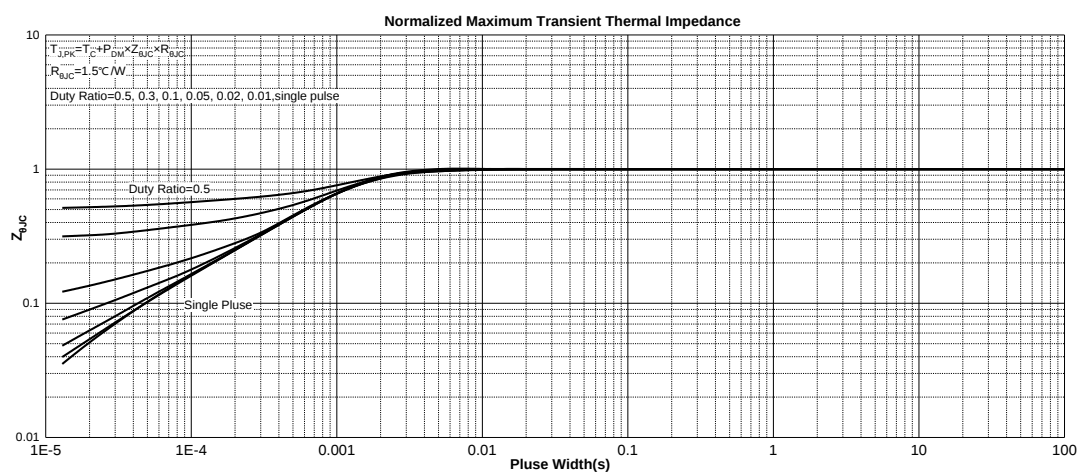
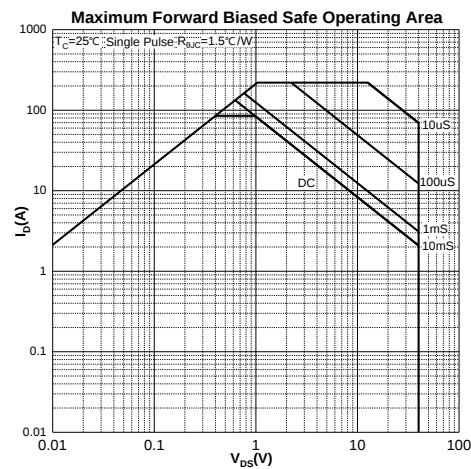
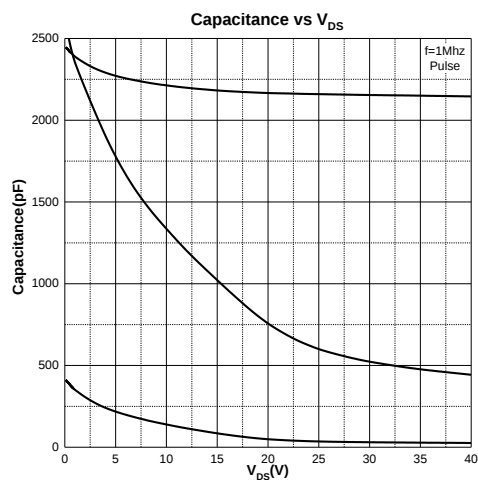
MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Off Characteristics						
Drain - Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V			1	μA
Gate - Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
On Characteristics ⁴						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	1.67	2.5	V
Drain-source On-resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 10A		3.3	4.5	mΩ
		V _{GS} = 4.5V, I _D = 10A		4.7	6.0	
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 10A		21		S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = 20V, V _{GS} = 0V, f = 1MHz		1579		pF
Output Capacitance	C _{oss}			572		
Reverse Transfer Capacitance	C _{rss}			38.5		
Gate Resistance	R _g	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz		0.57		Ω
Switching Characteristics						
Total Gate Charge	Q _g	V _{DS} = 20V, V _{GS} = 10V, I _D = 20A		31		nC
Gate-source Charge	Q _{gs}			6		
Gate-drain Charge	Q _{gd}			3.8		
Turn-on Delay Time	t _{d(on)}	V _{DD} = 20V, V _{GS} = 10V, R _L = 1Ω R _G = 3Ω		7		ns
Turn-on Rise Time	t _r			2.8		
Turn-off Delay Ttime	t _{d(off)}			24		
Turn-off Fall Time	t _f			3.9		
Source - Drain Diode Characteristics						
Diode Forward Voltage ⁴	V _{SD}	V _{GS} = 0V, I _S = 10A		0.73	1.2	V

Notes :

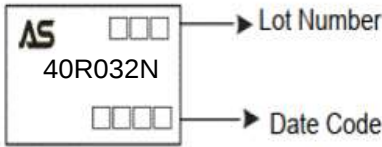
- 1.The maximum current rating is limited by package.And device mounted on a large heatsink
- 2.Pulse Test : Pulse Width $\leq 10\mu s$, duty cycle $\leq 1\%$.
- 3.EAS condition: $V_{DD} = 20V, V_{GS} = 10V, L = 0.5mH, R_G = 25\Omega$ Starting $T_J = 25^{\circ}\text{C}$.
- 4.Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
- 5.The power dissipation P_D is limited by $T_{J(MAX)} = 150^{\circ}\text{C}$.And device mounted on a large heatsink
- 6.Device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^{\circ}\text{C}$.

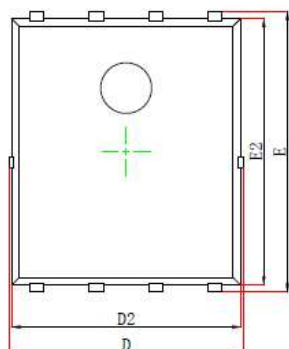




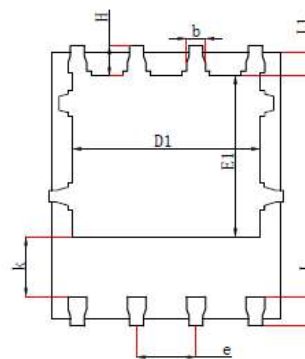
Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM40R032NQ-R	40R032N	DFN5*6-8	Tape&Reel	4000/Reel

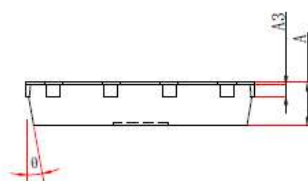
PACKAGE	MARKING
DFN5*6-8	 AS □□□□ → Lot Number 40R032N □□□□ → Date Code

DFN5x6_P, 8 Leads


Top View
[顶视图]



Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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