

Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

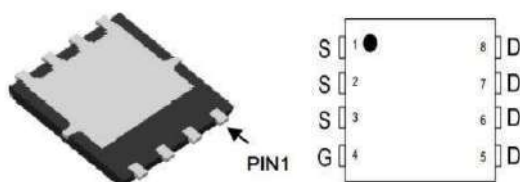
Application

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

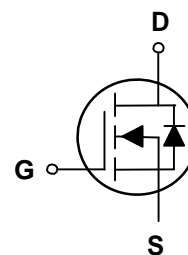


Product Summary

V_{DS}	40	V
$R_{DS(on),Max} @ V_{GS}=10\text{ V}$	1.5	$m\Omega$
I_D	120	A



PDFN5x6-8



■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current (Silicon limited)		I_D	200	A
Drain Current ^A	$T_C=25^\circ\text{C}$	I_D	120	A
	$T_C=100^\circ\text{C}$		82	
Pulsed Drain Current ^B		I_{DM}	360	A
Avalanche energy ^C		E_{AS}	450	mJ
Total Power Dissipation ^D		P_D	114	W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.1	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Ambient ^E		$R_{\theta JA}$	20	
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

■ Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	2.2		3.8	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A			1.5	mΩ
Gate Resistance	R _g	V _{GS} =0V,V _{DS} Open,f=1MHZ		2.7		Ω
Maximum Body-Diode Continuous Current	I _s				120	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V,f=300KHZ		9300		pF
Output Capacitance	C _{oss}			1410		
Reverse Transfer Capacitance	C _{rss}			78		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V,V _{DS} =32V,I _D =20A		127		nC
Gate-Source Charge	Q _{gs}			35		
Gate-Drain Charge	Q _{gd}			26		
Reverse Recovery Chrage	Q _{rr}	I _F =25A, di/dt=100A/us		163		ns
Reverse Recovery Time	t _{rr}			100		
Turn-on Delay Time	t _{d(on)}	V _{GS} =10V,V _{DD} =20V,I _D =25A R _{GEN} =2Ω		22.5		
Turn-on Rise Time	t _r			6.7		
Turn-off Delay Time	t _{d(off)}			80.3		
Turn-off fall Time	t _f			26.9		

Note:

- The maximum current rating is package limited.
- Repetitive rating; pulse width limited by max. junction temperature.
- $V_{DD}=32V, R_G=25\Omega, L=0.5\text{mH}$, starting $T_J=25^{\circ}\text{C}$.
- P_D is based on max. junction temperature, using junction-case thermal resistance.
- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25^{\circ}\text{C}$.

■ Typical Performance Characteristics

Figure.1 Typical Output Characteristics

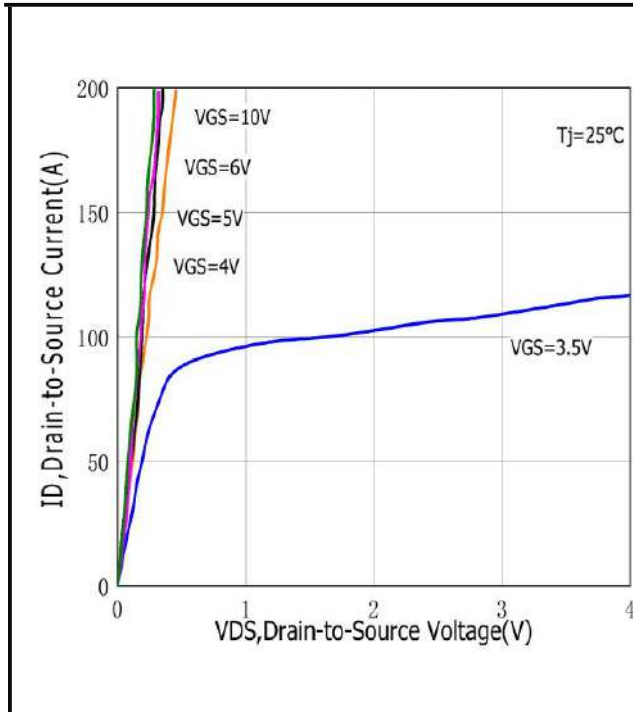


Figure.2 Typical Gate Charge vs Gate to Source Voltage

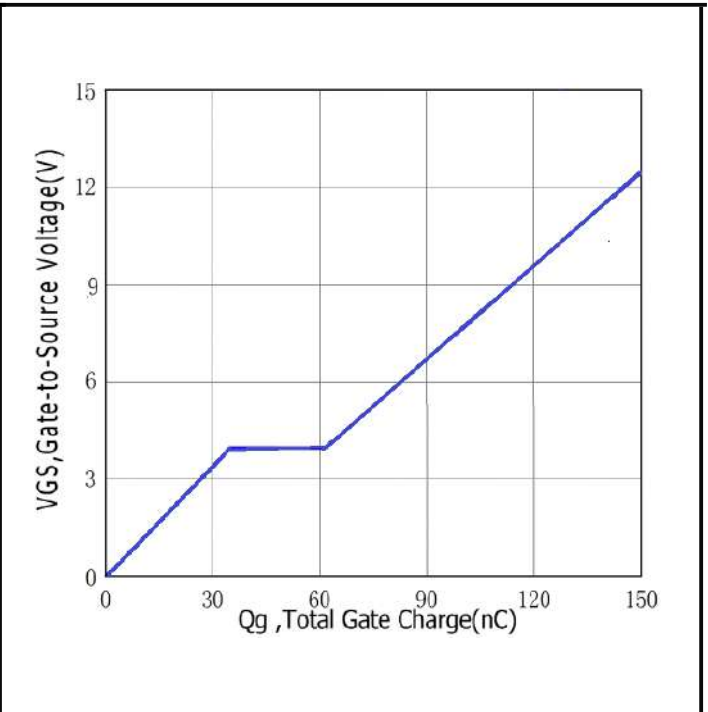


Figure.3 Typical Body Diode Transfer Characteristics

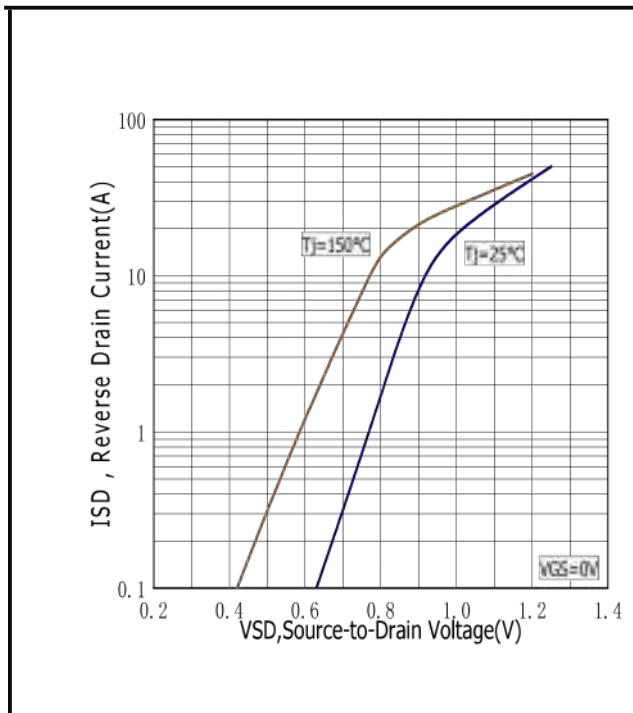
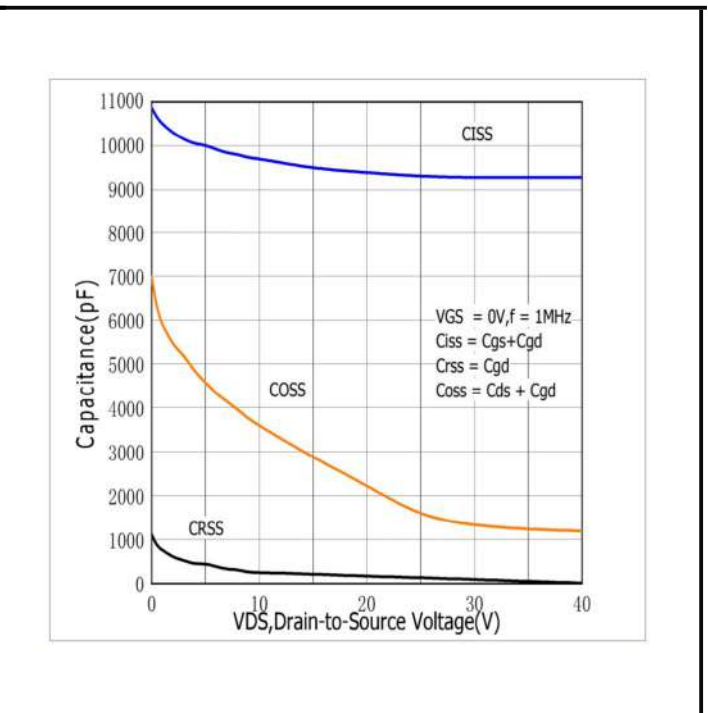


Figure.4 Typical Capacitance vs Drain to Source Voltage



■ Typical Performance Characteristics

Figure.5 Typical Breakdown Voltage vs Junction Temperature

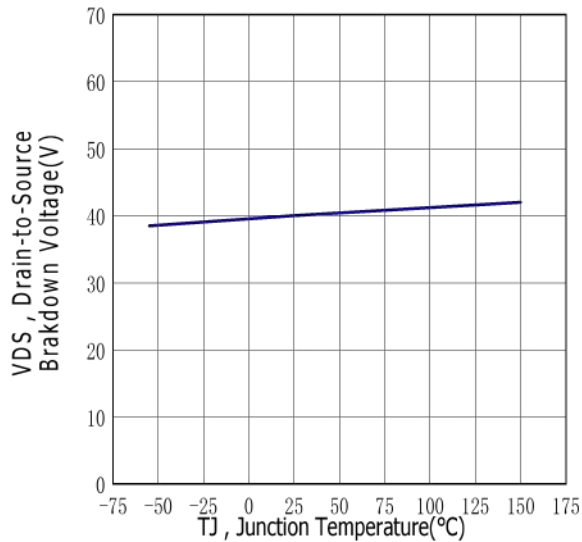


Figure.6 Typical Drain to Source on Resistance vs Junction Temperature

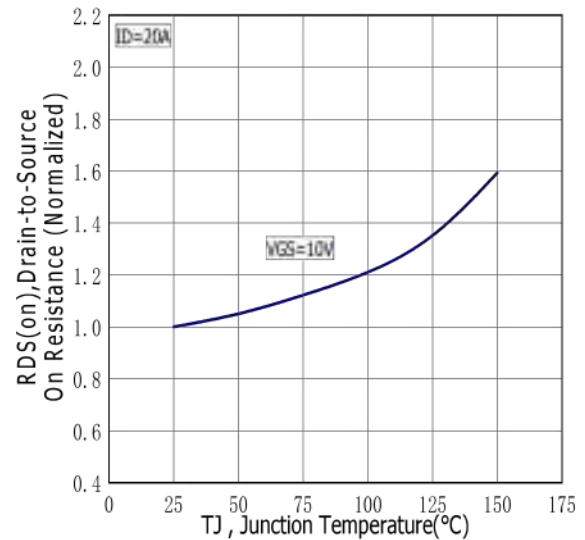


Figure.7 Maximum Forward Bias Safe Operating Area

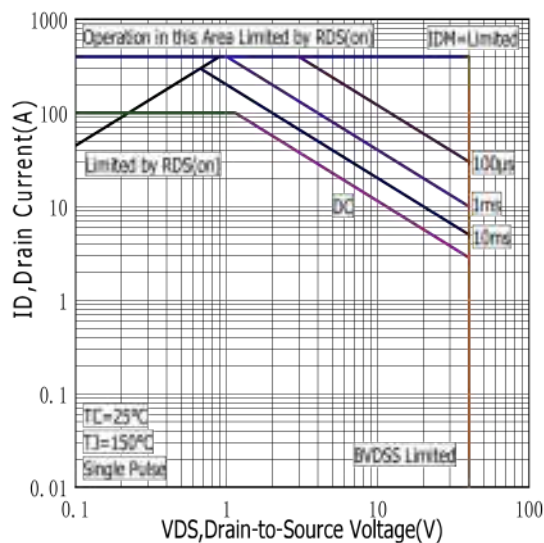
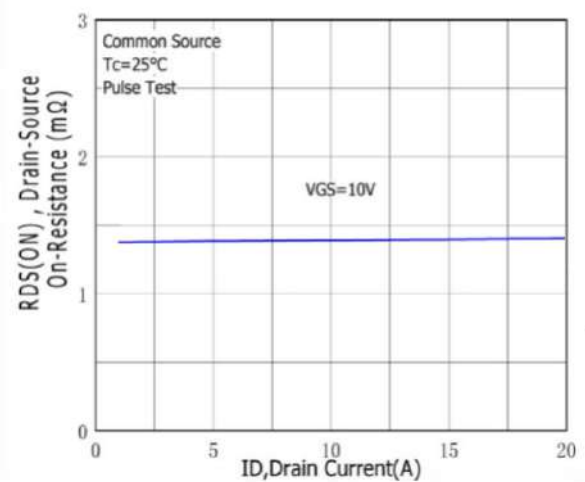


Figure.8 Typical Drain to Source ON Resistance vs Drain Current



■ Typical Performance Characteristics

Figure.9 Maximum EAS vs Channel Temperature

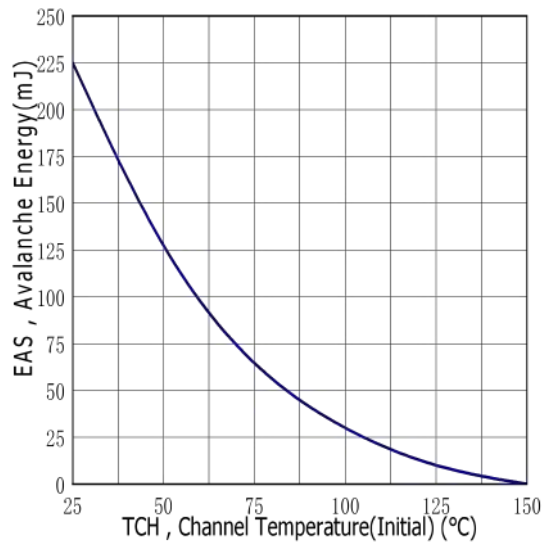


Figure.10 Typical Threshold Voltage vs Case Temperature

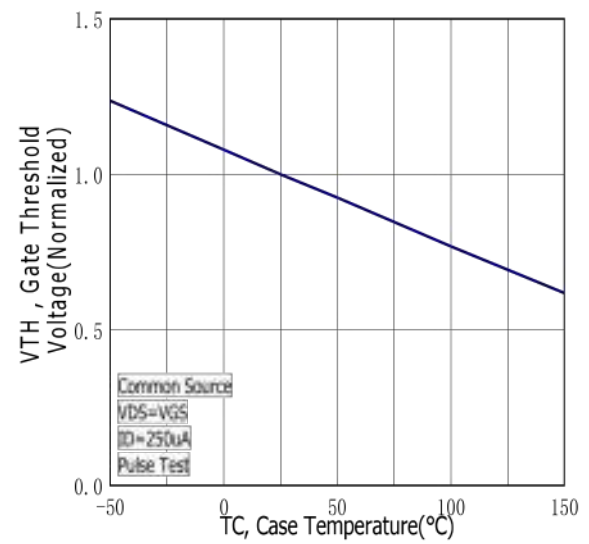


Figure.11 Typical Transfer Characteristics

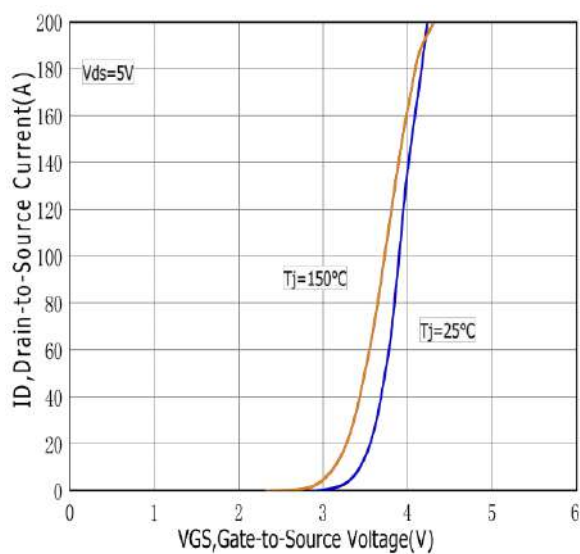


Figure.12 Maximum Power Dissipation vs Case Temperature

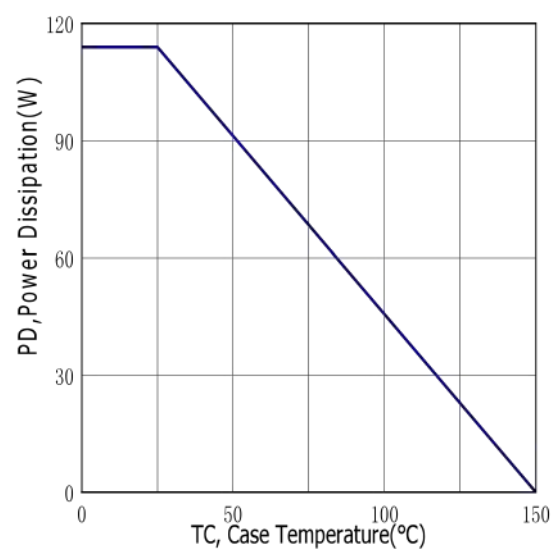
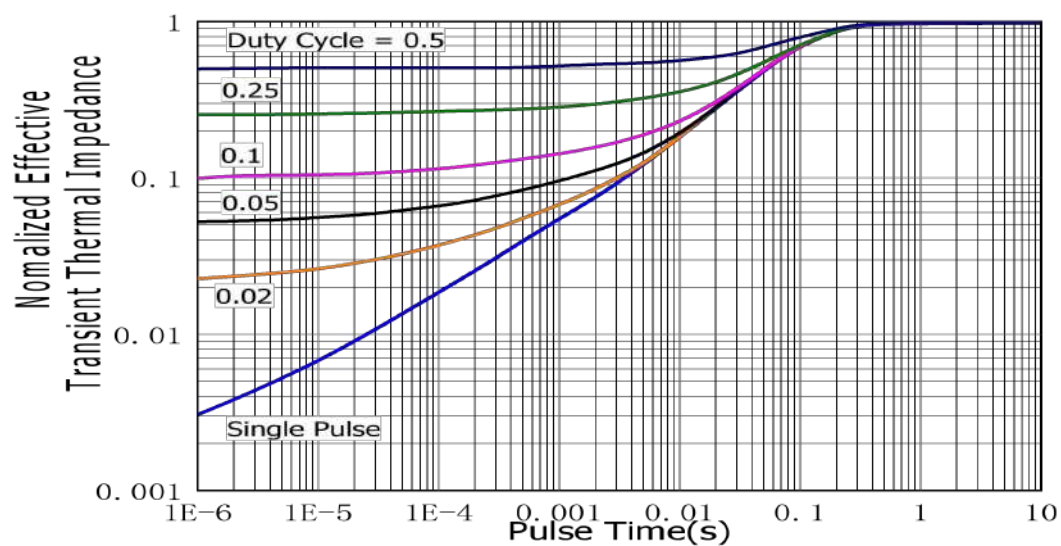


Figure.13 Maximum Effective Thermal Impedance , Junction to Case



■ Test circuits and waveforms

Figure A: Gate Charge Test Circuit & Waveforms

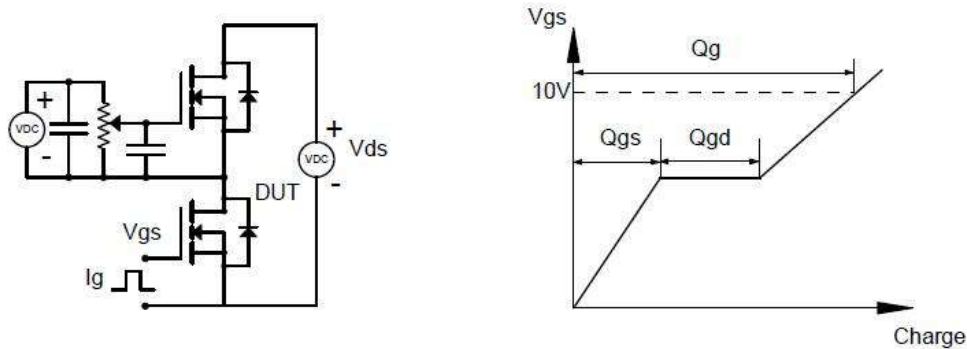


Figure B: Resistive Switching Test Circuit & Waveforms

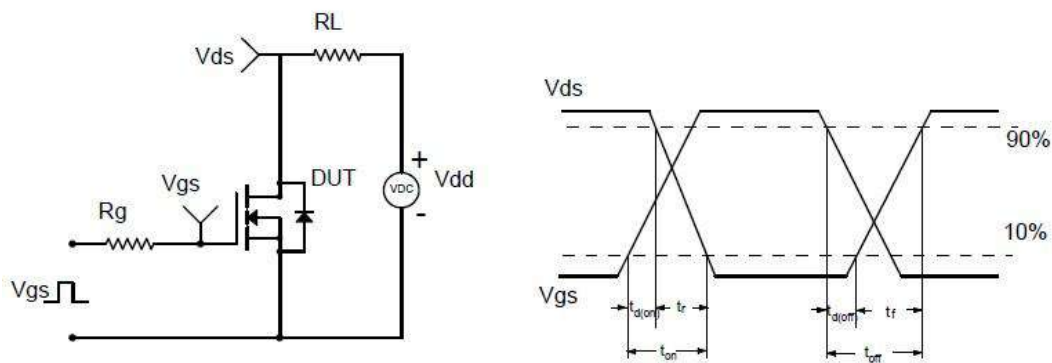


Figure C: Unclamped Inductive Switching (UIS) Test

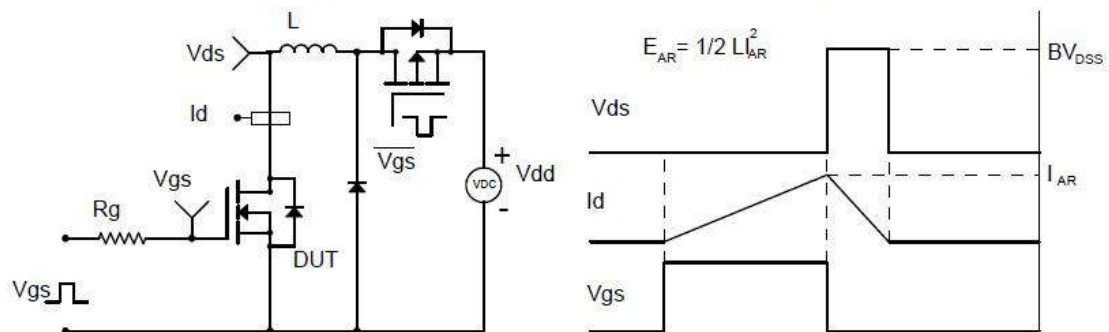
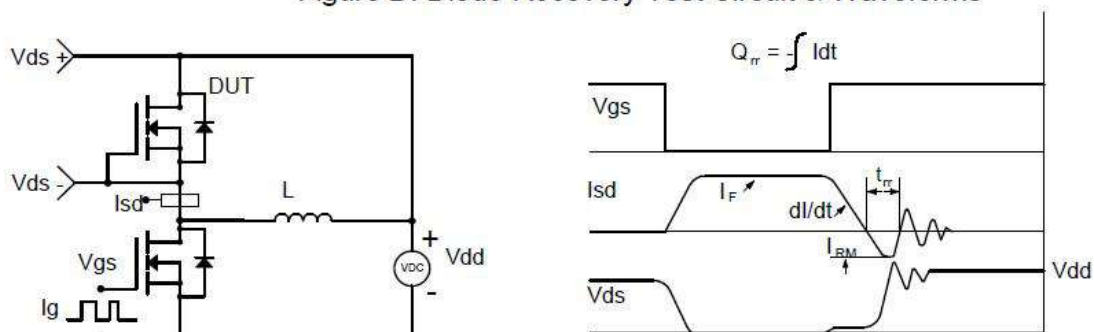
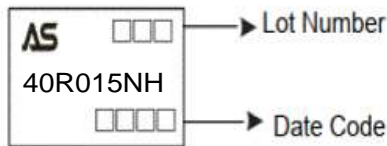


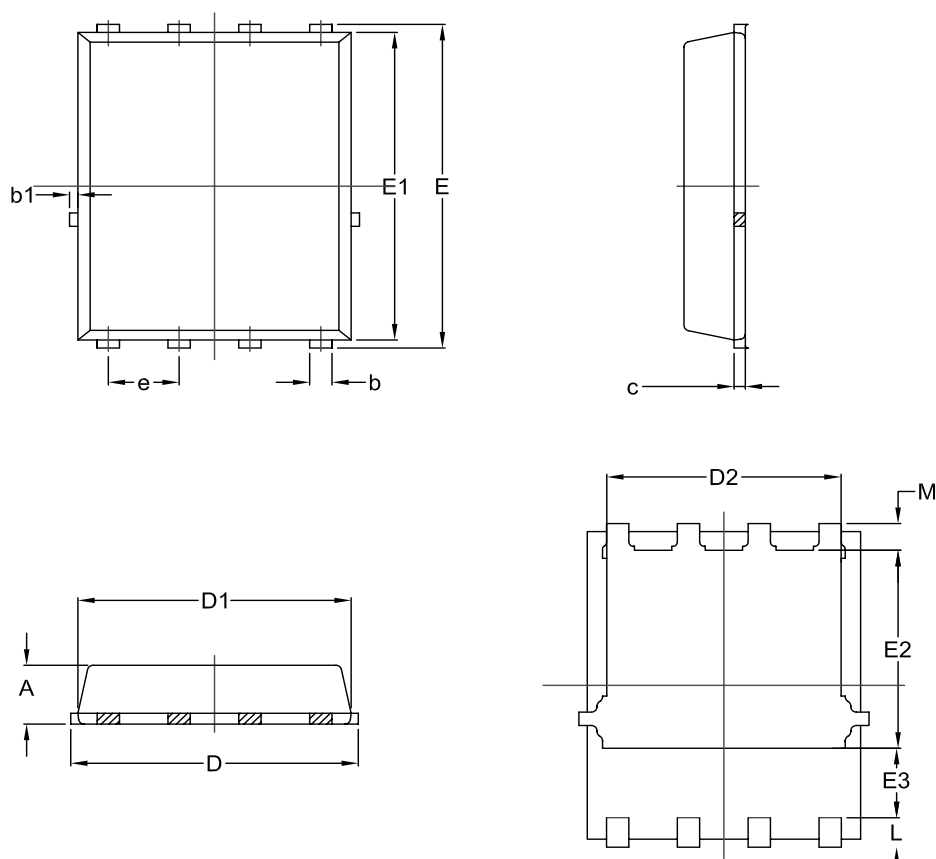
Figure D: Diode Recovery Test Circuit & Waveforms



Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM40R015NHQ-R	40R015NH	PDFN5*6-8	Tape&Reel	4000/Reel

PACKAGE	MARKING
PDFN5*6-8	 <p>AS □□□ → Lot Number</p> <p>40R015NH</p> <p>□□□□ → Date Code</p>


Notes:

1.Dimension D1 ,E1 not included mold flash

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.00	1.10	1.20
b	0.30	0.40	0.50
b1	0.02	0.15	0.22
c	0.15	0.20	0.35
D	4.95	5.25	5.45
D1	4.80	4.90	5.00
D2	4.00	4.20	4.40
E	5.95	6.05	6.25
E1	5.65	5.75	5.85
E2	3.30	3.60	3.90
E3	1.10	/	/
e	1.27		
L	0.38	0.55	0.70
M	0.35	0.50	0.65

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