



General Features

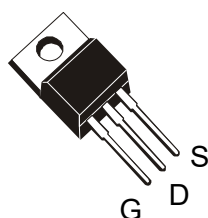
- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Application

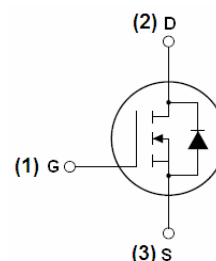
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Product Summary

V_{DS}	80	V
$R_{DS(on), Typ @ V_{GS}=10V}$	5.4	mΩ
I_D	110	A



TO-220 top view



Absolute Maximum Ratings at T=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	80	V
V_{GS}	Gate-Source Voltage	±20	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	110	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	105	A
I_{DM}	Pulsed Drain Current ²	270	A
EAS	Single Pulse Avalanche Energy ³	300	mJ
I_{AS}	Avalanche Current	34	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation ⁴	56	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	55	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	0.84	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	80	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=20A$	---	5.4	6	$m\Omega$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V$, $I_D=20A$	---	---	8.5	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	2.5	---	3.4	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=64V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=64V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	1	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V$, $I_D=20A$	---	75	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	1.2	---	Ω
Qg	Total Gate Charge (10V)	$V_{DS}=40V$, $V_{GS}=10V$, $I_D=20A$	---	40	---	nC
Qgs	Gate-Source Charge		---	7.2	---	
Qgd	Gate-Drain Charge		---	6.5	---	
Td(on)	Turn-On Delay Time	$V_{DD}=40V$, $V_{GS}=10V$, $R_G=3\Omega$, $I_D=20A$	---	8.3	---	ns
Tr	Rise Time		---	4.2	---	
Td(off)	Turn-Off Delay Time		---	36	---	
Tf	Fall Time		---	6.9	---	
Ciss	Input Capacitance	$V_{DS}=40V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	3730	---	pF
Coss	Output Capacitance		---	674	---	
Crss	Reverse Transfer Capacitance		---	24.24	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	48	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=A$, $T_J=25^\circ\text{C}$	---	0.7	---	V
t_{rr}	Reverse Recovery Time	$I_F=20A$, $dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	27	---	nS
Q_{rr}	Reverse Recovery Charge		---	89	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=34A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 6.The maximum current rating is package limited.

Test Circuit

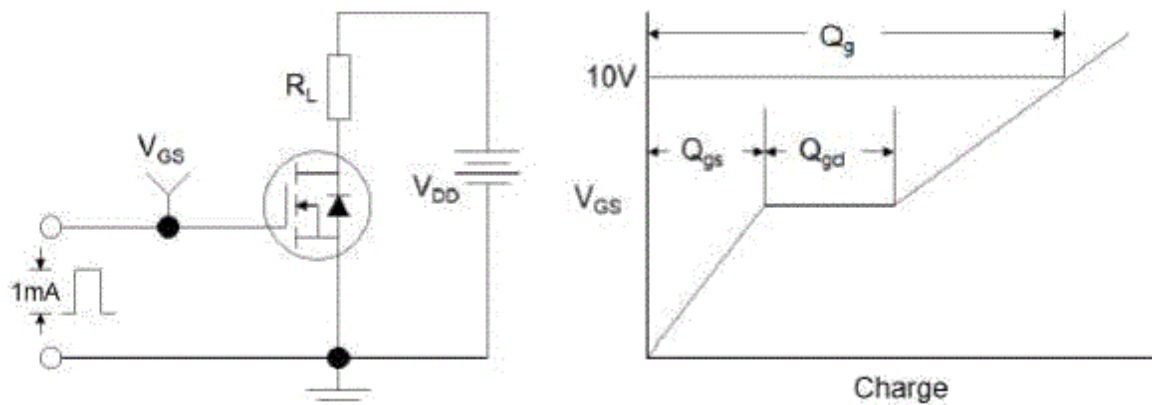


Figure1:Gate Charge Test Circuit & Waveform

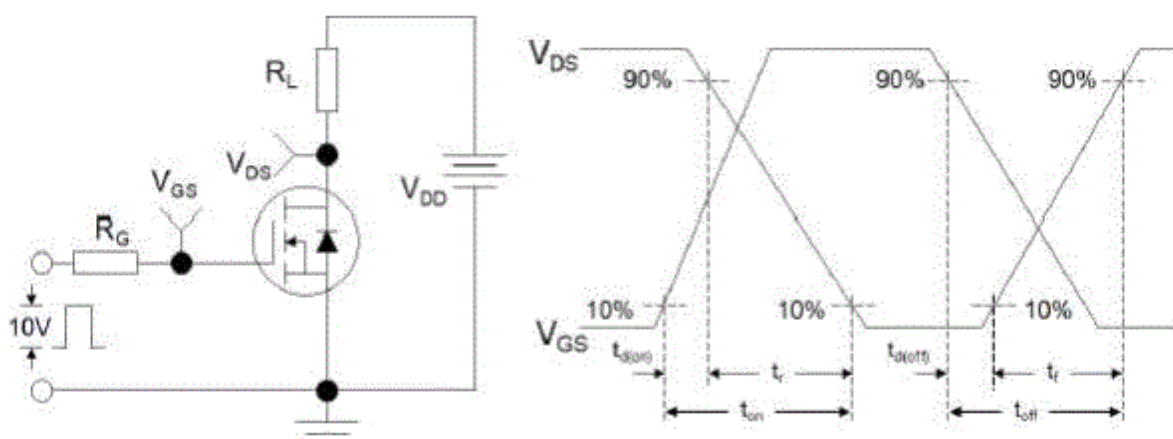


Figure 2: Resistive Switching Test Circuit & Waveforms

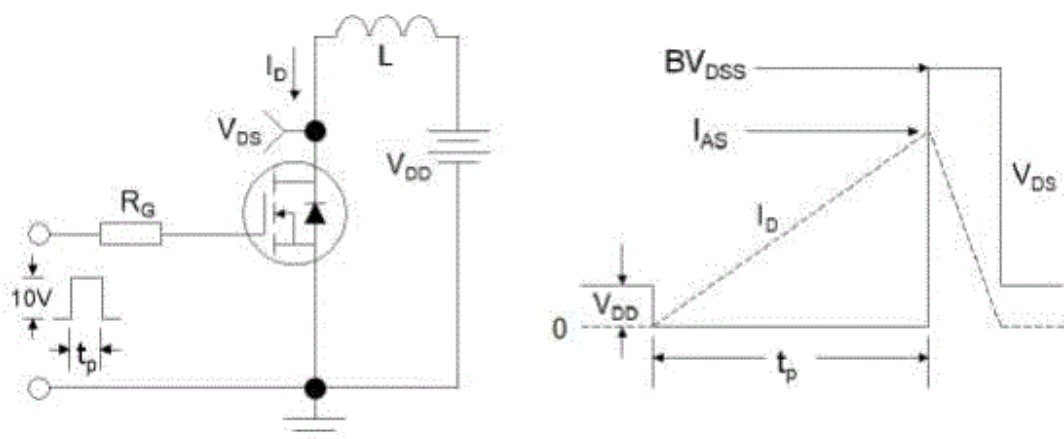


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Typical Characteristics

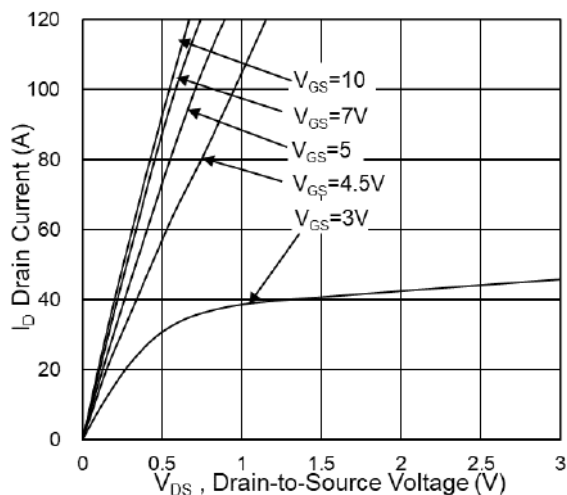


Fig.1 Typical Output Characteristics

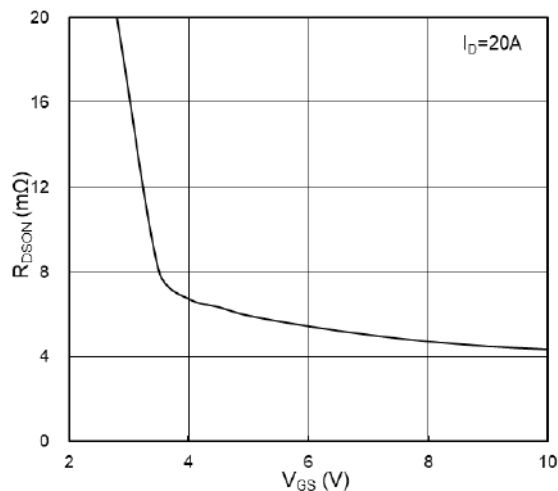


Fig.2 On-Resistance vs G-S Voltage

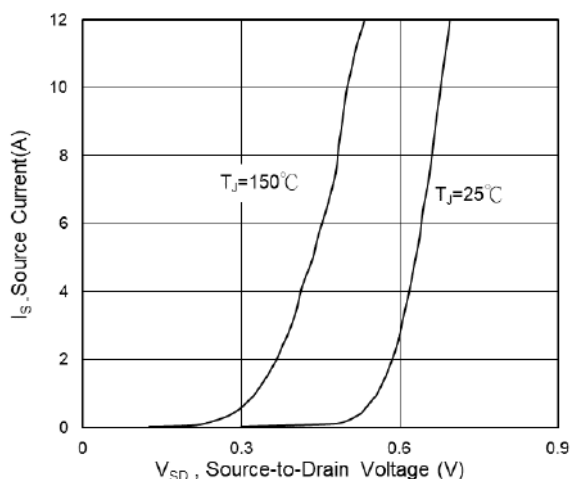


Fig.3 Source Drain Forward Characteristics

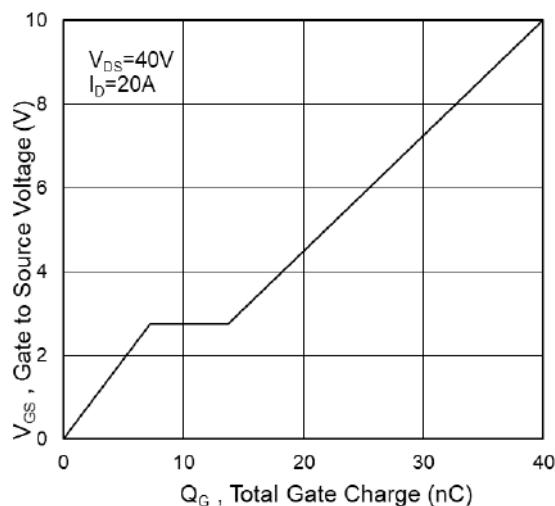


Fig.4 Gate-Charge Characteristics

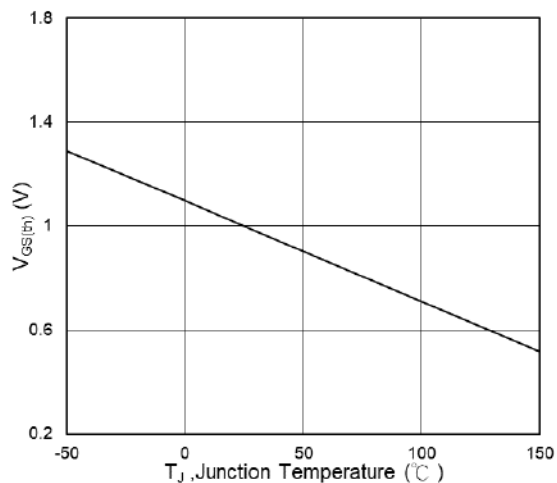


Fig.5 Normalized $V_{GS(th)}$ vs T_J

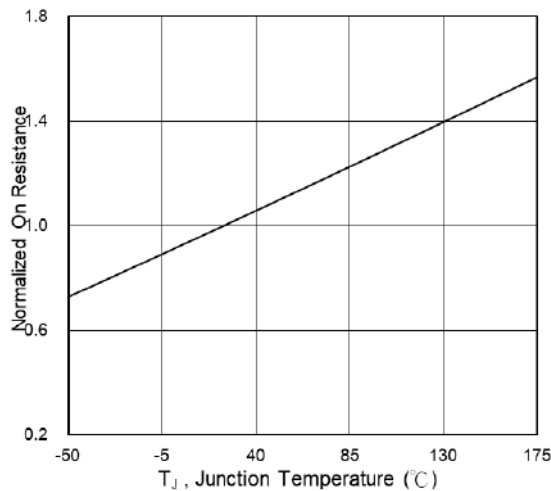


Fig.6 Normalized $R_{DS(on)}$ vs T_J

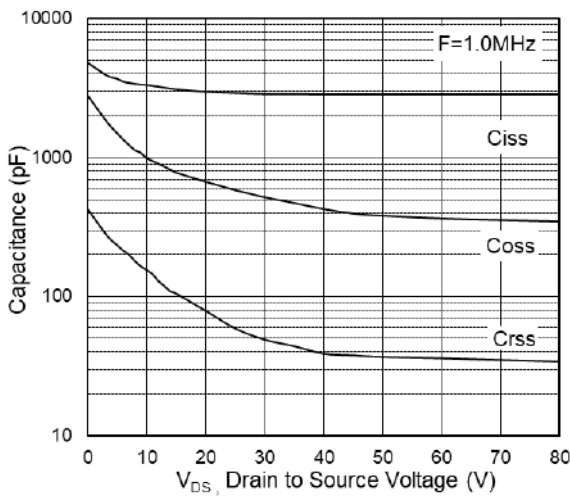


Fig.7 Capacitance

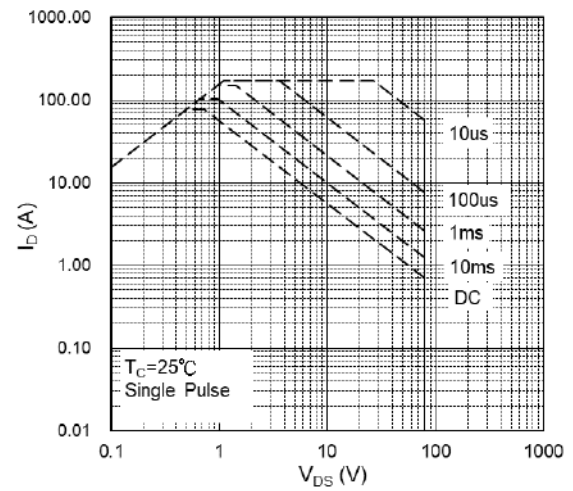


Fig.8 Safe Operating Area

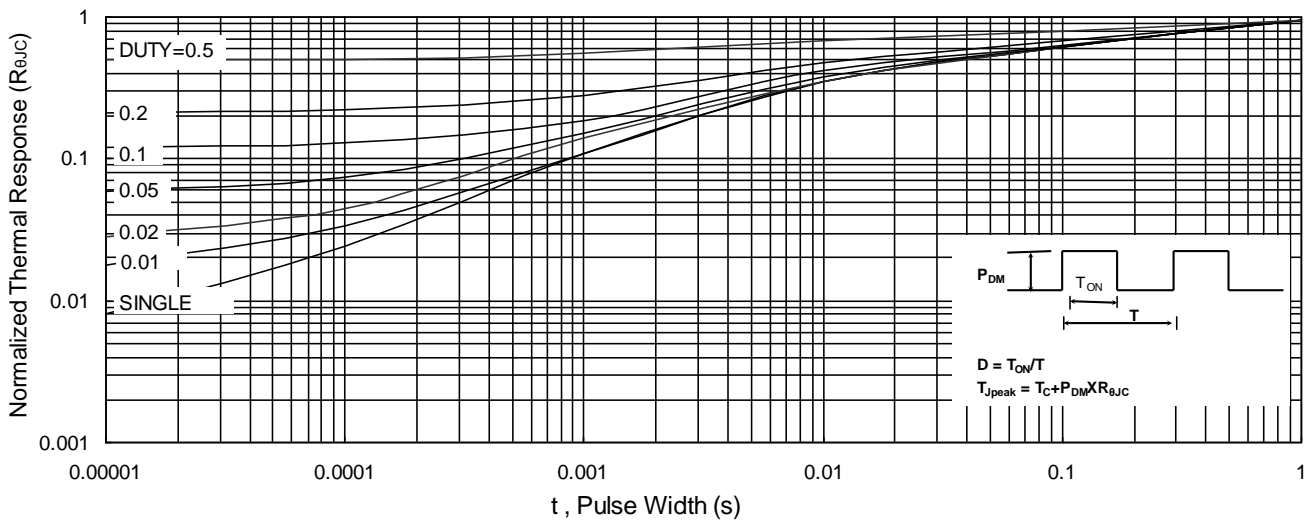


Fig.9 Normalized Maximum Transient Thermal Impedance

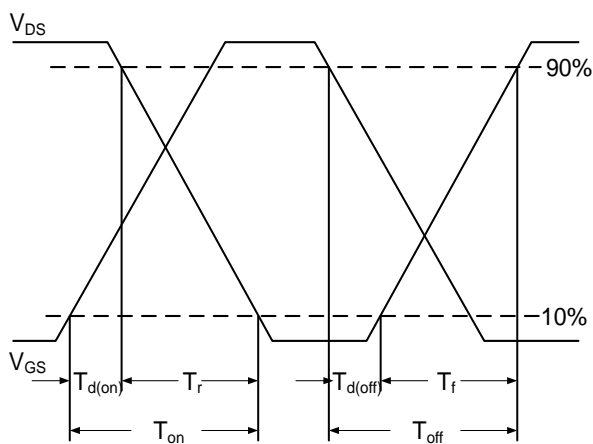


Fig.10 Switching Time Waveform

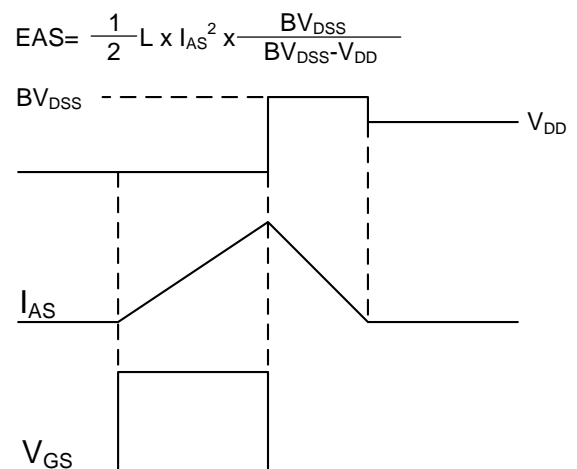
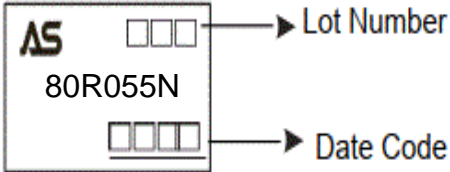


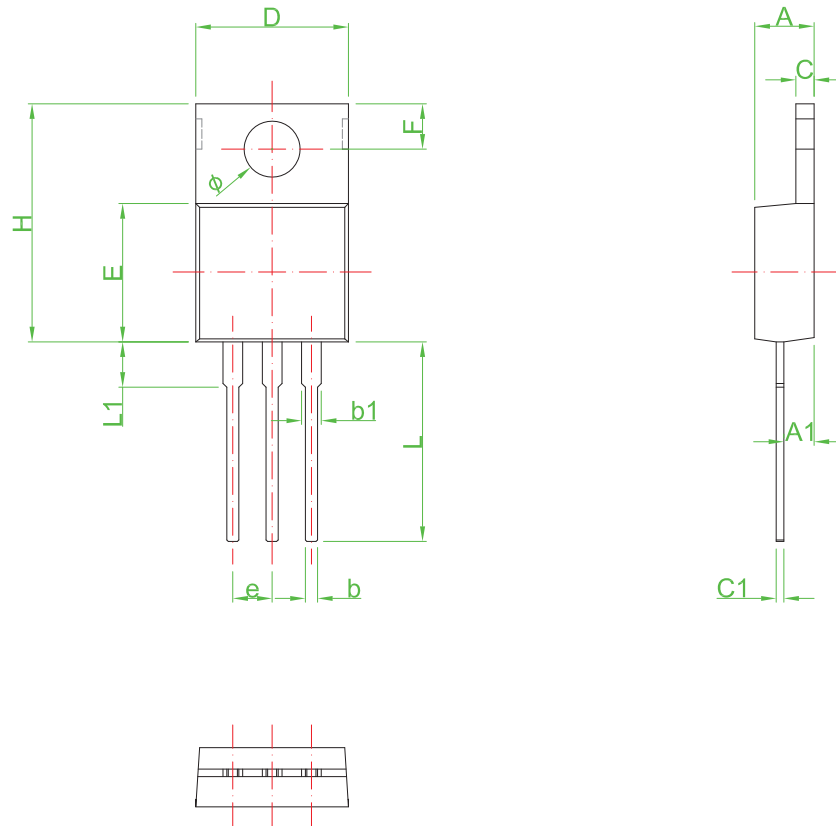
Fig.11 Unclamped Inductive Switching Waveform

Ordering and Marking Information

Ordering Device No	Marking	Package	Packing	Quantity
ASDM80R055NP-T	80R055N	TO-220	Tube	50/Tube

PACKAGE	MARKING
TO-220	 <p>The diagram shows a TO-220 package with the following markings: <ul style="list-style-type: none"> AS (Ascend Semi logo) 80R055N (Part number) Lot Number (indicated by two empty boxes) Date Code (indicated by four empty boxes) </p>

TO-220 Package Information



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	4.00	4.80	0.157	0.189
A1	1.80	2.80	0.071	0.110
b	0.60	1.00	0.024	0.039
b1	1.14	1.78	0.045	0.070
C	1.00	1.40	0.039	0.055
C1	0.36	0.61	0.014	0.024
D	9.90	10.50	0.390	0.413
E	8.38	9.20	0.330	0.362
e	2.54 TYP		0.100 TYP	
F	2.54	3.20	0.100	0.126
∅	3.50	3.90	0.138	0.154
H	14.48	15.87	0.570	0.625
L	13.00	13.80	0.512	0.543
L1	---	4.10	---	0.161

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