Features

◇ High Speed Power Switching, Logic Level
◇ Enhanced Body diode dv/dt capability
◇ Enhanced Avalanche Ruggedness
◇ 100% UIS Tested, 100% Rg Tested
◇ Lead Free, Halogen Free

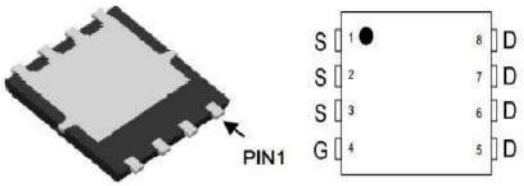
Product Summary

RoHS

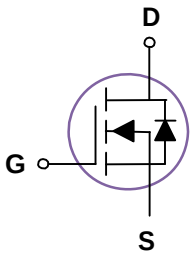
V_{DS}	100	V
$R_{DS(on),Typ}$@ V_{GS}=10 V	7.3	mΩ
I_D	55	A

Application

◇ Synchronous Rectification in SMPS
◇ Hard Switching and High Speed Circuit
◇ DC/DC in Telecoms and Inductrial



DFN5×6-8



Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	55	A
		T_C=100℃	38	
Drain to Source Voltage	V_{DS}	-	100	V
Gate to Source Voltage	V_{GS}	-	+20/-12	V
Pulsed Drain Current	I_{DM}	-	80	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.1mH, T_C=25℃	80	mJ
Power Dissipation	P_D	T_C=25℃	3.1	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Lead	$R_{\theta JL}$	23	℃/W
Thermal Resistance Junction-Ambient (t≤10s)	$R_{\theta JA}$	40	℃/W
Thermal Resistance Junction-Ambient (steady state)		75	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Static Characteristics						
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	100	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	1.8	2.5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=95V, T_j=25℃	-	-	1	μA
		V_{GS}=0V, V_{DS}=95V, T_j=125℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=14A	-	7.3	9	mΩ
		V_{GS}=4.5V, I_D=10A	-	11	12	
Transconductance	g_{fs}	V_{DS}=5V, I_D=14A	-	70	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.5	-	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V, f=1MHz	-	3350	-	pF
Output Capacitance	C_{oss}		-	270	-	
Reverse Transfer Capacitance	C_{rss}		-	15	-	
Total Gate Charge	Q_g(10V)	V_{DD}=50V, I_D=14A, V_{GS}=10V	-	49	-	nC
Total Gate Charge	Q_g(4.5V)		-	21	-	
Gate to Source Charge	Q_{gs}		-	8	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	7	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=50V, I_D=14A, V_{GS}=10V, R_G=10Ω,	-	10	-	ns
Rise time	t_r		-	5	-	
Turn off Delay Time	$t_{d(off)}$		-	32	-	
Fall Time	t_f		-	6	-	
Reverse Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=14A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=50V, I_F=14A, dI_F/dt=500A/μs	-	47	-	ns
Reverse Recovery Charge	Q_{rr}		-	226	-	nC

Fig 1. Typical Output Characteristics

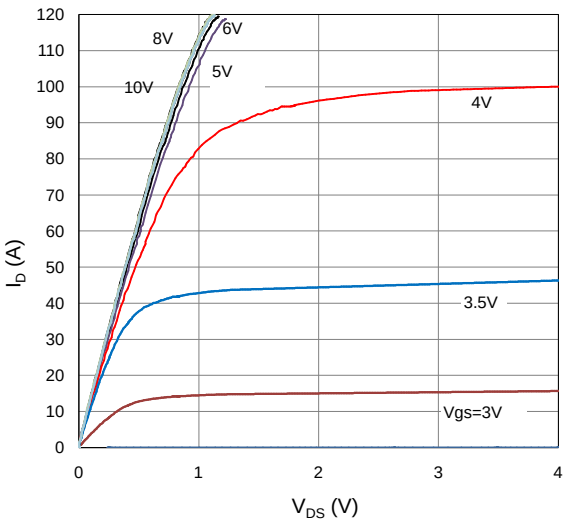


Figure 2. On-Resistance vs. Gate-Source Voltage

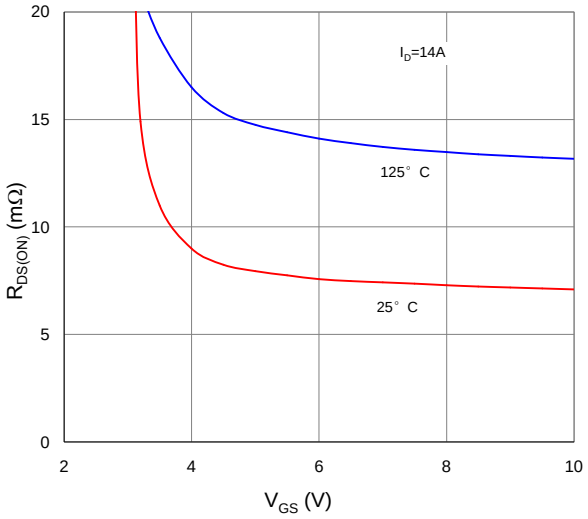


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

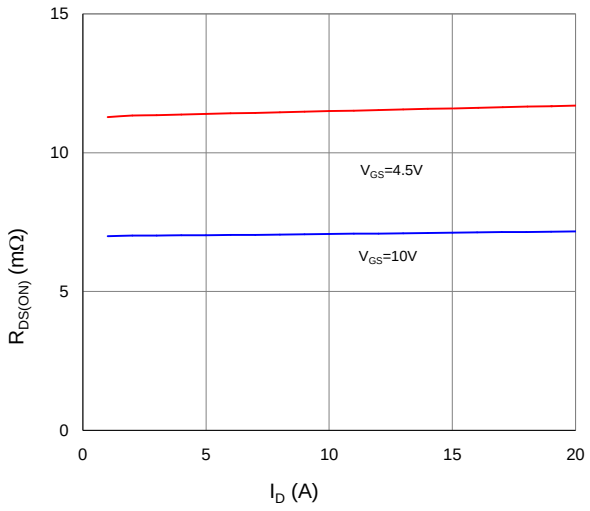


Figure 4. Normalized On-Resistance vs. Junction Temperature

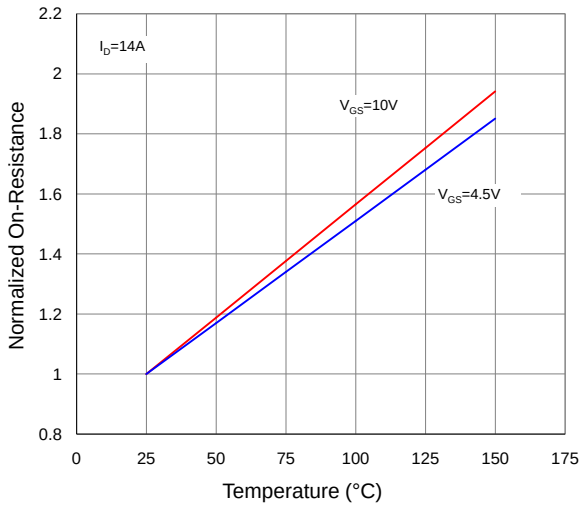


Figure 5. Typical Transfer Characteristics

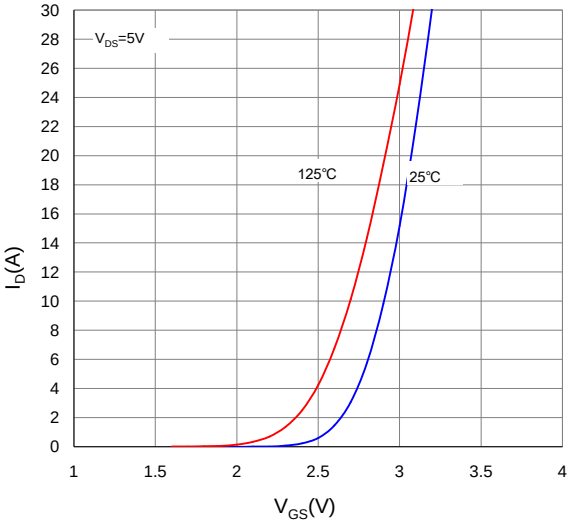


Figure 6. Typical Source-Drain Diode Forward Voltage

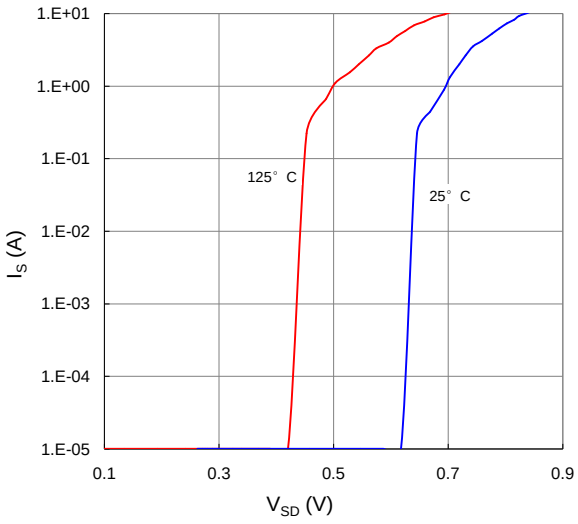


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

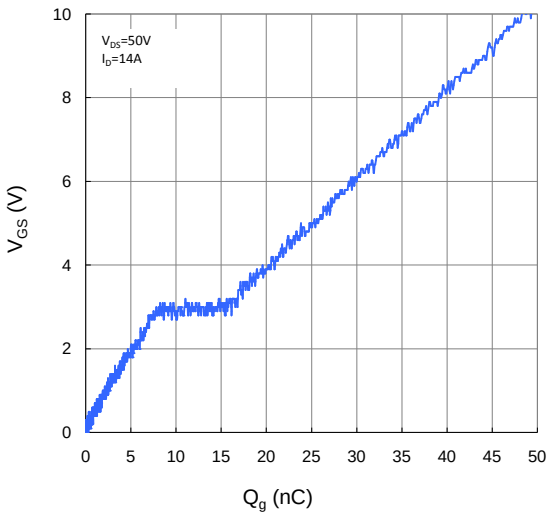


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

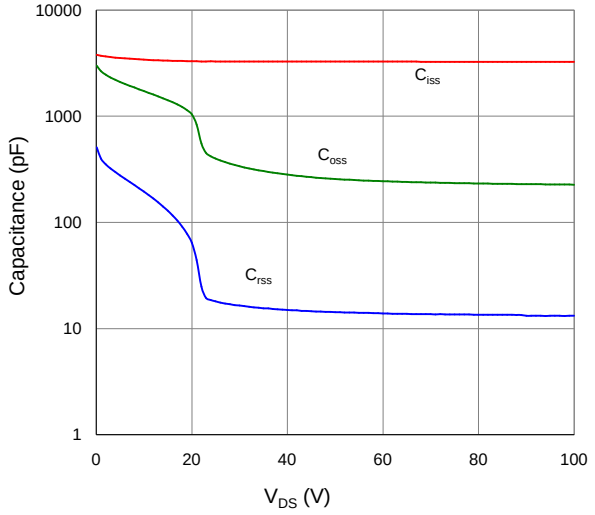


Figure 9. Maximum Safe Operating Area

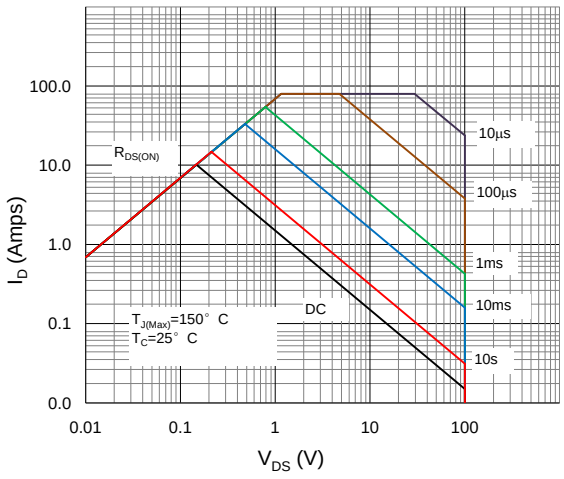


Figure 10. Maximun Drain Current vs. Case Temperature

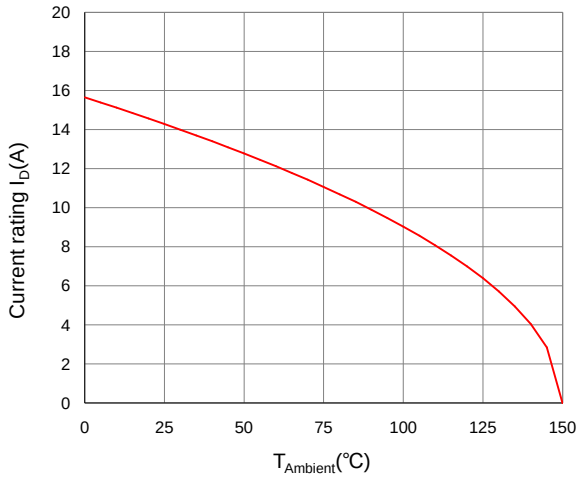
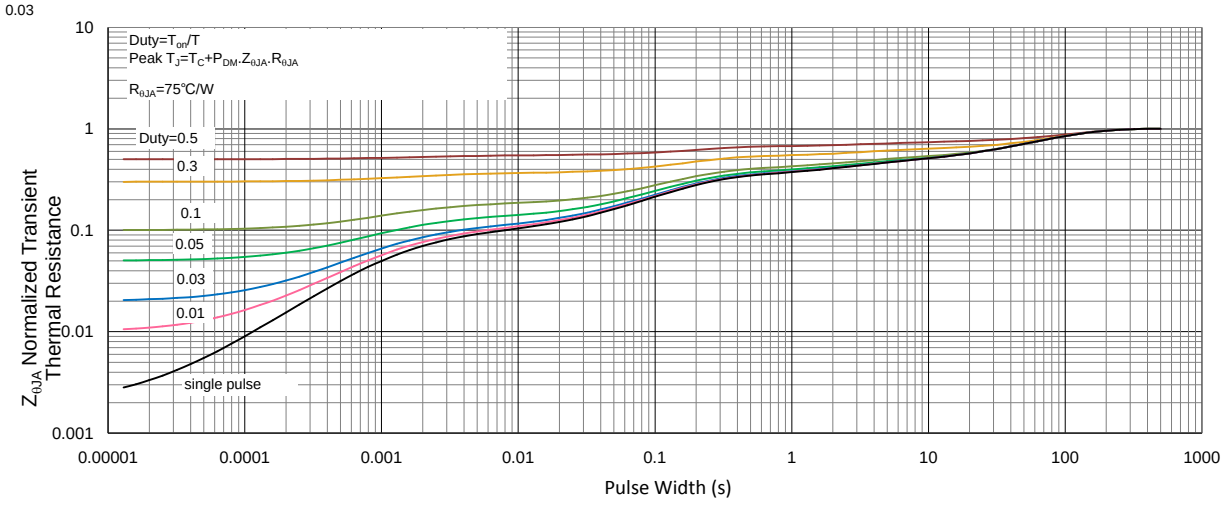
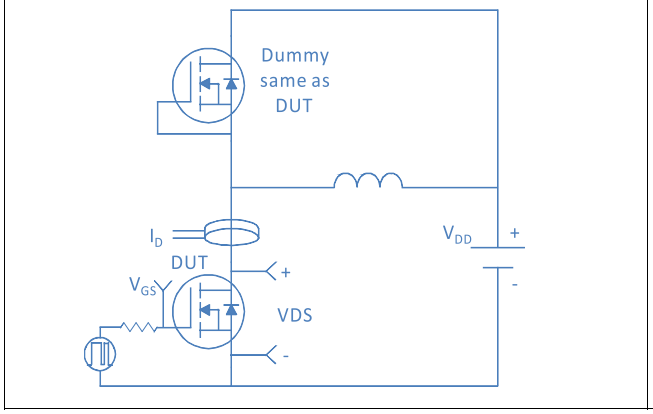
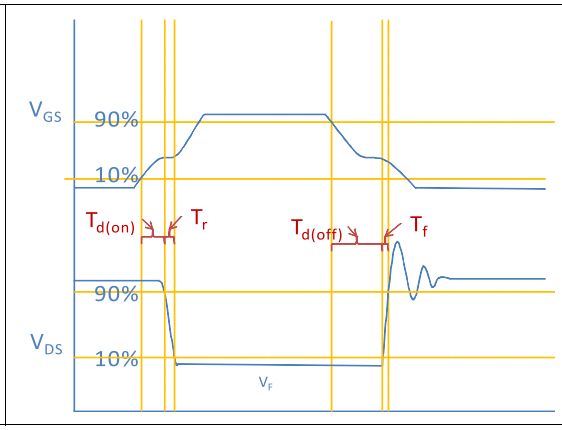


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

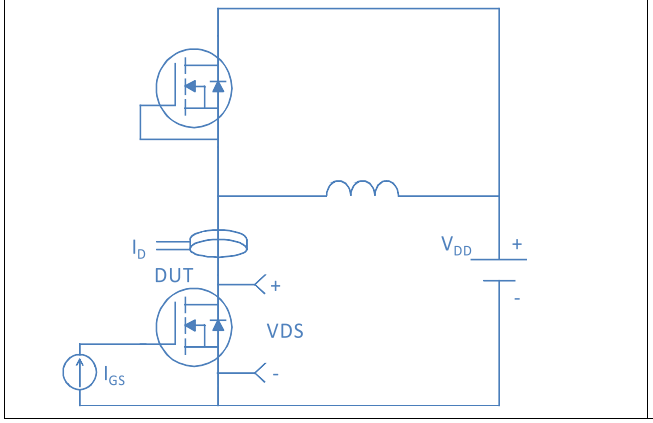


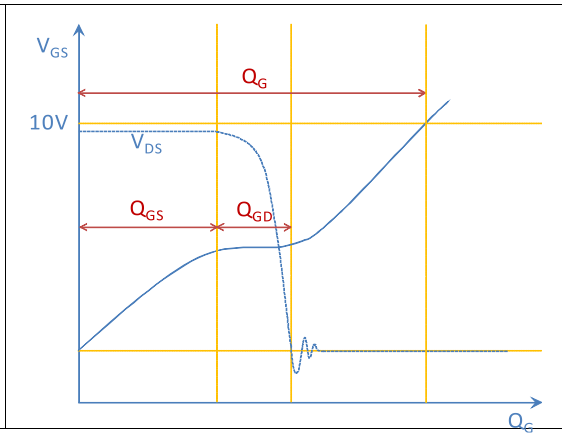
Inductive switching Test



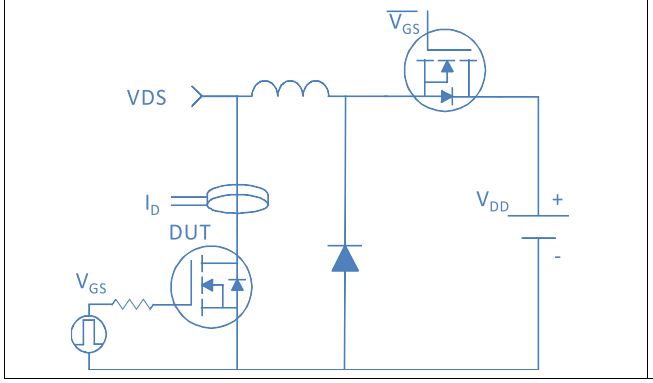


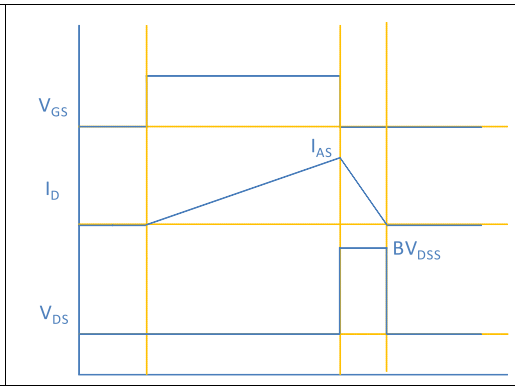
Gate Charge Test



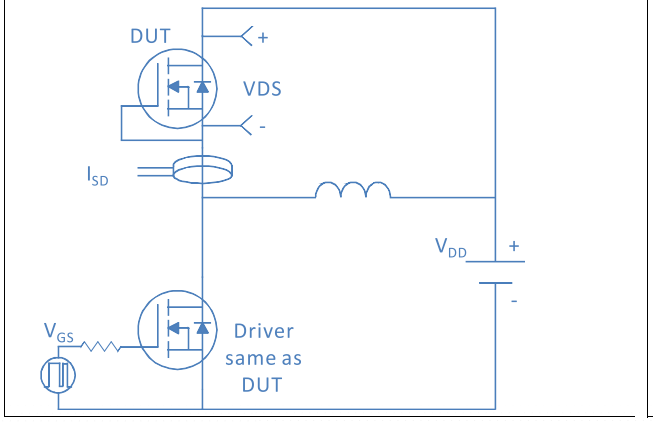


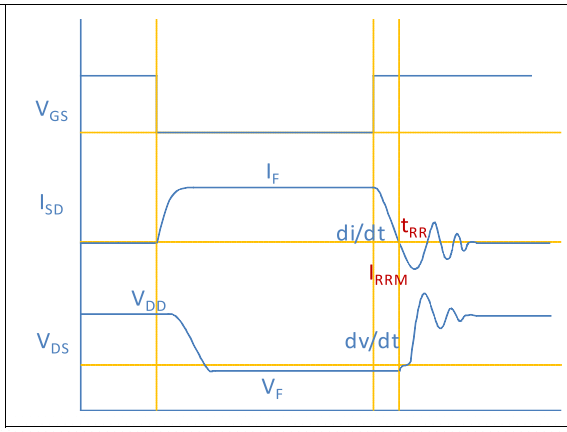
Uclamped Inductive Switching (UIS) Test





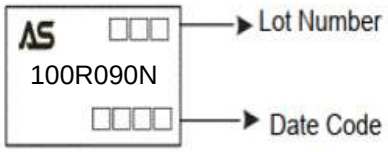
Diode Recovery Test



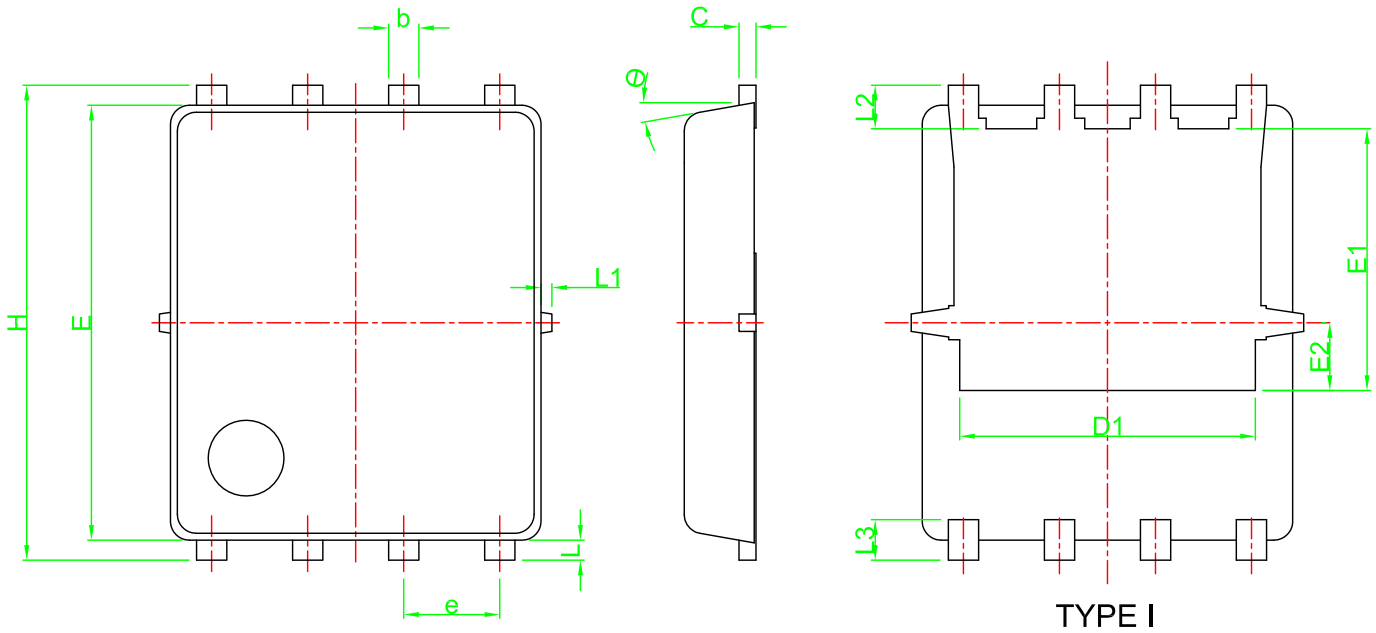


Ordering and Marking Information

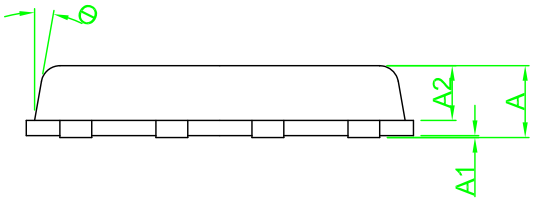
Ordering Device No.	Marking	Package	Packing	Quantity
ASDM100R090NQ-R	100R090N	DFN5*6-8	Tape&Reel	4000/Reel

PACKAGE	MARKING
DFN5*6-8	

DFN5*6-8 PACKAGE IN FORMATION



TYPE I



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.85	1.00	0.033	0.039
A1	0.01	0.05	0.000	0.002
A2	0.69	0.75	0.027	0.030
b	0.40	0.45	0.016	0.018
C	0.20	0.30	0.008	0.012
D	4.80	4.95	0.189	0.195
D1	3.91	4.06	0.154	0.160
e	1.27 TYP		0.05 TYP	
E	5.65	5.80	0.222	0.228
E1	3.46	3.50	0.136	0.138
E2	0.80	0.95	0.031	0.037
L	0.15	0.3	0.006	0.012
L1	0.08	0.15	0.003	0.006
L2	0.58	0.73	0.023	0.029
L3	0.45	0.60	0.018	0.024
H	6.15	6.28	0.242	0.247
Θ	8°	12°	8°	12°

IMPORTANT NOTICE

ShenZhen Ascend Semiconductor incorporated MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

ShenZhen Ascend Semiconductor Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. ShenZhen Ascend Semiconductor Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does ShenZhen Ascend Semiconductor Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume .

all risks of such use and will agree to hold Ascendsemi Incorporated and all the companies whose products are represented on ShenZhen Ascend Semiconductor Incorporated website, harmless against all damages.

ShenZhen Ascend Semiconductor Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use ShenZhen Ascend Semiconductor Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold ShenZhen Ascend Semiconductor Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

www.ascendsemi.com