Features

- 2.5V to 5.5V Input Voltage Range
- 2A Continuous Output Current
- 1.2MHz Switching Frequency
- Built-in Short Protection
- Built-in Over Current Limit
- Built-in Over Voltage Protection
- PFM Mode for High Efficiency in Light Load
- High Efficiency: Up to 96%
- Internal Soft-Start
- Output Adjustable from 0.6V
- Over Temperature Protected
- Low Quiescent Current: 40μA
- Available in SOT23-5 package
- -40°C to +85°C Temperature Range

Applications

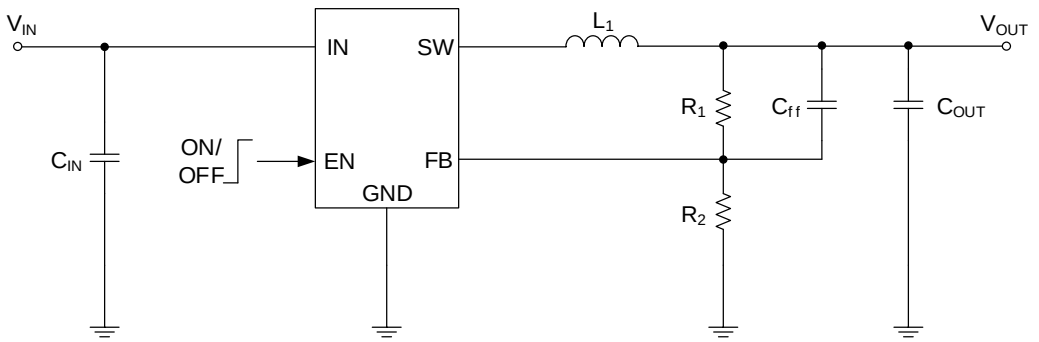
- Cellular and Smart Phones
- Wireless and DSL Modems
- PDAs
- Portable Instruments
- Digital Still and Video Cameras
- PC Cards

General Description

The ASP3420 is a high-efficiency monolithic synchronous buck regulator using a constant frequency, current mode architecture. The device is available in an adjustable version. The 2.5V to 5.5V input voltage range makes the ASP3420 ideally suited for single Li-Ion battery powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems. PWM/PFM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally set at 1.2MHz, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.6V feedback reference voltage.

The ASP3420 requires a minimal number of readily available, external components and is available in a space saving SOT23-5 package.

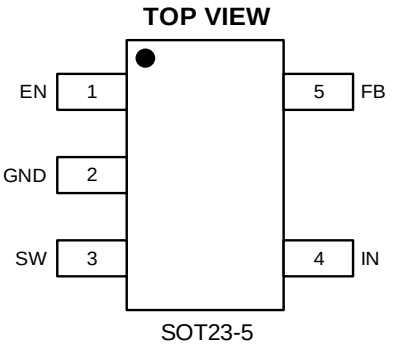
Typical Application Circuit



Basic Application Circuit

Pin Description

Pin Configuration



Top Marking: ADYLL (device code: AD, Y=year code, LL= lot number code)

Pin Description

Pin	Name	Function
1	EN	Chip Enable Pin. Drive EN above 1.2V to turn on the part. Drive EN below 0.6V to turn it off. Do not leave EN floating.
2	GND	Ground Pin.
3	SW	Power Switch Output. It is the switch node connection to Inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches.
4	IN	Power Supply Input. Must be closely decoupled to GND with a 10μF or greater ceramic capacitor.
5	FB	Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.

Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V_{IN} voltage	-0.3	6.5	V
EN voltage	-0.3	6.5	V
SW voltage (While Switch, AC, less than 10ns)	-5	8	V
FB voltage	-0.3	6	V
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	-55	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD\text{-}HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD\text{-}CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH\text{-}UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	-40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	2.5	5.5	V
Output current	0	2	A

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	130	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board.

Electrical Characteristics (1)(2)

V_{IN}=5V, T_A=25°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range		2.5		5.5	V
Supply Current (Quiescent)	V_{EN} =3.0V		40	80	μA
Supply Current (Shutdown)	V_{EN} =0 or EN = GND		0.1	1.0	μA
Feedback Voltage		0.585	0.600	0.615	V
High-Side Switch On-Resistance	I_{SW}=100mA		80		mΩ
Low-Side Switch On-Resistance	I_{SW}=-100mA		50		mΩ
Upper Switch Current Limit		3			A
Over Voltage Protection Threshold			6.2		V
Switching Frequency			1.2		MHz
EN Rising Threshold		1.2			V
EN Falling Threshold				0.6	V
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage		2.5		V
	Shutdown V_{IN} Voltage	1.8	1.9		V
	Hysteresis V_{IN} voltage		600		mV
Soft Start			1		mS
Thermal Shutdown			160		℃
Thermal Hysteresis			30		℃

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

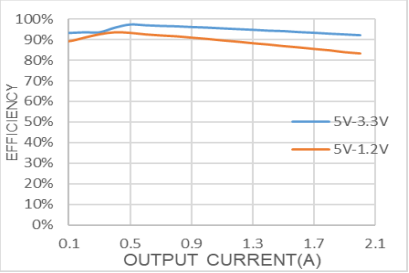
Typical Performance Characteristics (1)(2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): V_{IN} =5V, V_{OUT}=3.3V, T_A = +25ºC, unless otherwise noted.

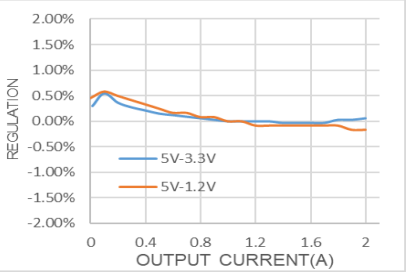
Efficiency vs Load Current

V_{IN}=5V, V_{OUT}=3.3V/1.2V



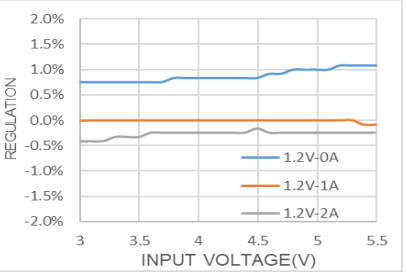
Load Regulation

V_{IN}=5V, V_{OUT}=3.3V/1.2V



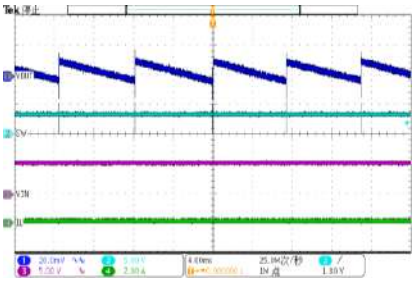
Line Regulation

V_{IN}=5V, V_{OUT}=1.2V, I_{OUT}=0A/1A/2A



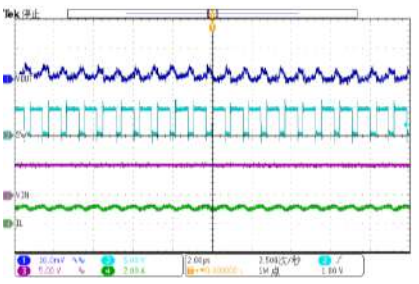
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



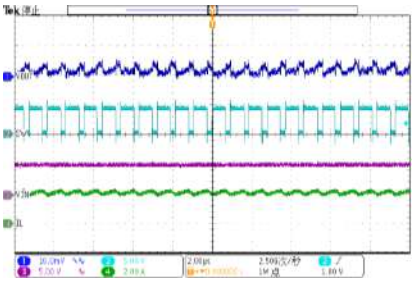
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A



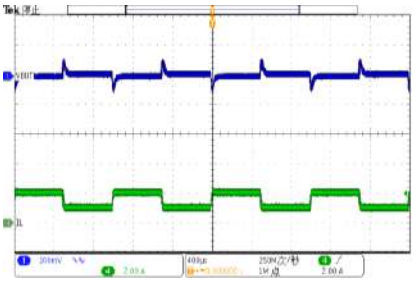
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=2A



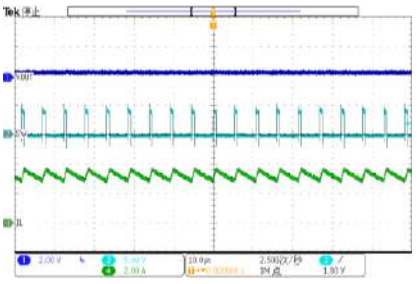
Loop Response

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=1A-2A



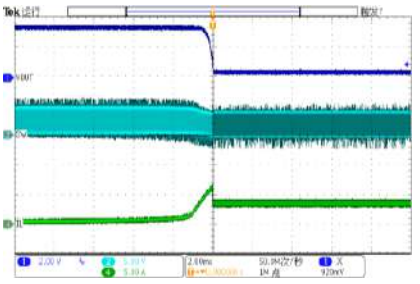
Output Short

V_{IN}=5V, V_{OUT}=3.3V



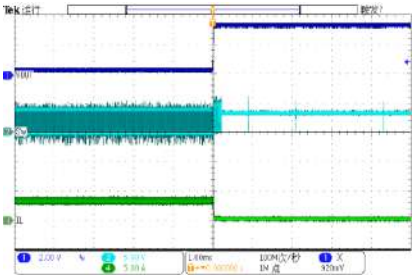
Short Circuit Entry

V_{IN}=5V, V_{OUT}=3.3V



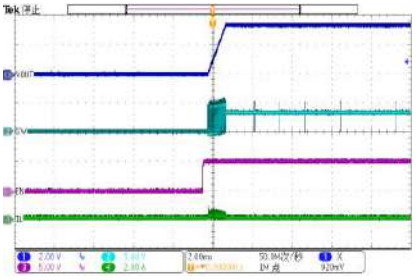
Short Circuit Recovery

V_{IN}=5V, V_{OUT}=3.3V



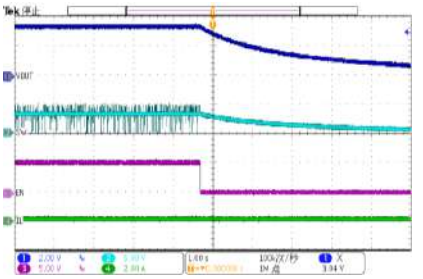
Enable Startup at No Load

V_{IN}=5V, V_{OUT}=3.3V



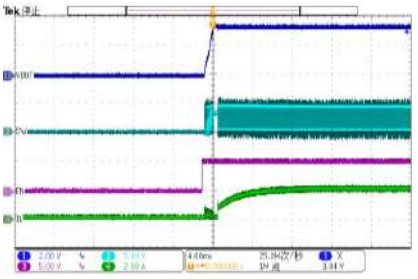
Enable Shutdown at No Load

V_{IN}=5V, V_{OUT}=3.3V



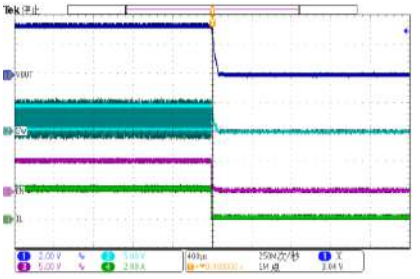
Enable Startup at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=2A



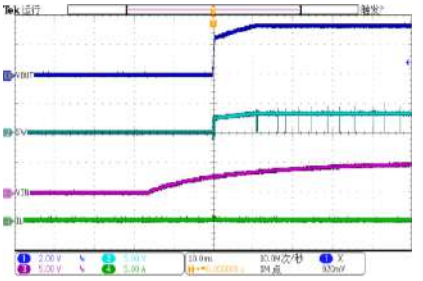
Enable Shutdown at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=2A



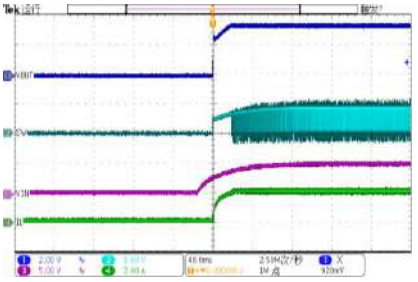
Power Up at No Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A

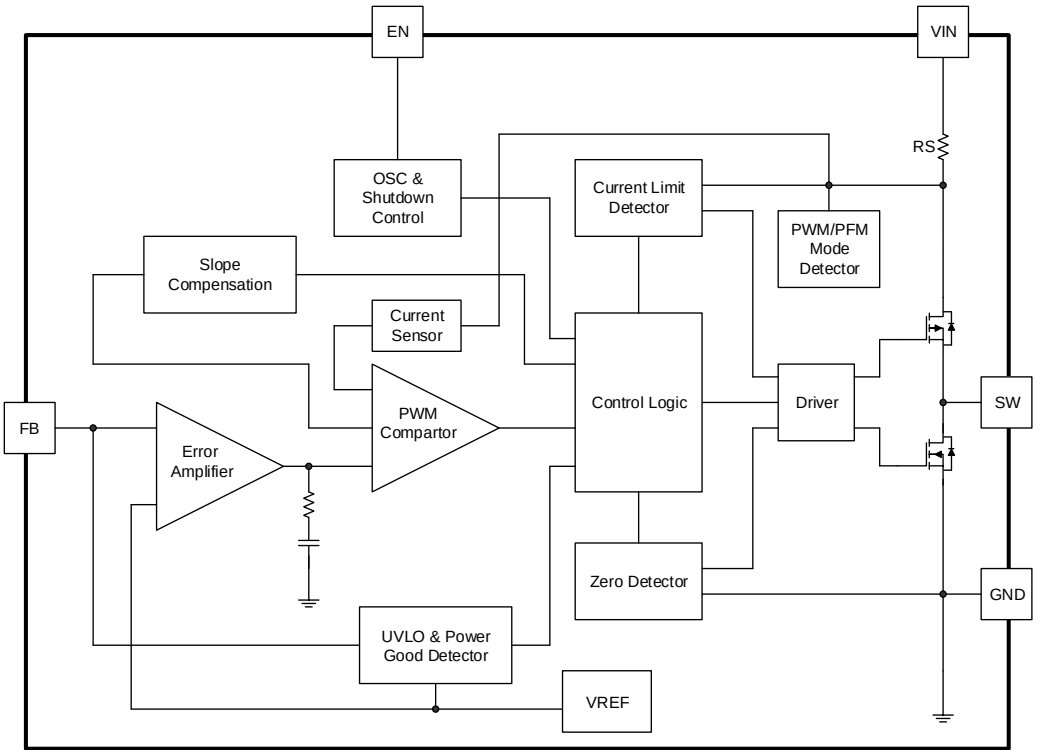


Power Up at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=2A



Functional Block Diagram



Block Diagram

Functions Description

Internal Regulator

The ASP3420 is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.2MHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally to 1ms.

Startup and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Applications Information

Setting the Output Voltage

ASP3420 require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. ASP3420 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 100kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	L1(μH)	C_{IN}(μF)	C_{OUT}(μF)	C_{FF} (pF) Opt.
1.0	6.667	10	2.2	22	22×2	C_{FF} Chapter
1.05	7.500	10	2.2	22	22×2	C_{FF} Chapter
1.2	10.000	10	2.2	22	22×2	C_{FF} Chapter
1.5	15.000	10	2.2	22	22×2	C_{FF} Chapter
1.8	20.000	10	3.3	22	22×2	C_{FF} Chapter
2.5	31.667	10	3.3	22	22×2	C_{FF} Chapter
3.3	45.000	10	4.7	22	22×2	C_{FF} Chapter

All the external components are the suggested values, the final values are based on the application testing results.

Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the maximum inductor peak current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. The inductor value

can be calculated with:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% to 40% of the maximum load current. The maximum inductor peak current can be estimated as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency. Larger inductances lead to smaller ripple currents and voltages, but they also have larger physical dimensions, lower saturation currents and higher linear impedance. Therefore, the choice of inductance should be compromised according to the specific application.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For a better performance, use ceramic capacitors placed as close to VIN as possible and a 0.1μF input capacitor to filter out high frequency interference is recommended. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

From the above equation, it can be concluded that the input ripple current reaches its maximum at V_{IN}=2V_{OUT} where $I_{CIN} = \frac{I_{OUT}}{2}$. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimate with Equation:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Similarly, when V_{IN}=2V_{OUT}, input voltage ripple reaches its maximum of $\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$.

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

There are some differences between different types of capacitors. In the case of ceramic capacitors, the impedance

at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times {F_{OSC}}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A larger output capacitor can achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value (C_{OUT_MAX}) can be limited approximately with Equation:

$$C_{OUT\_MAX} = \left(I_{LIM\_AVG} - I_{OUT}\right) \times T_{SS}/V_{OUT}$$

Where L_{LIM_AVG} is the average start-up current during the soft-start period, and T_{SS} is the soft- start time.

On the other hand, special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Feed-Forward Capacitor (C_{FF})

ASP3420 has internal loop compensation, so adding C_{FF} is optional. Specifically, for specific applications, if necessary, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (C_{FF}) in the feedback network is to improve the transient response or higher phase margin. For optimizing the feed-forward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feed-forward capacitor identified, the value of feed-forward capacitor (C_{FF}) can be calculated with the following Equation:

$$C_{FF} = \frac{1}{2\pi \times F_{CROSS}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

PC Board Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the V_{IN} Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. $V_{OUT,}$ SW away from sensitive analog areas such as FB.

Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

Ordering and Marking Information

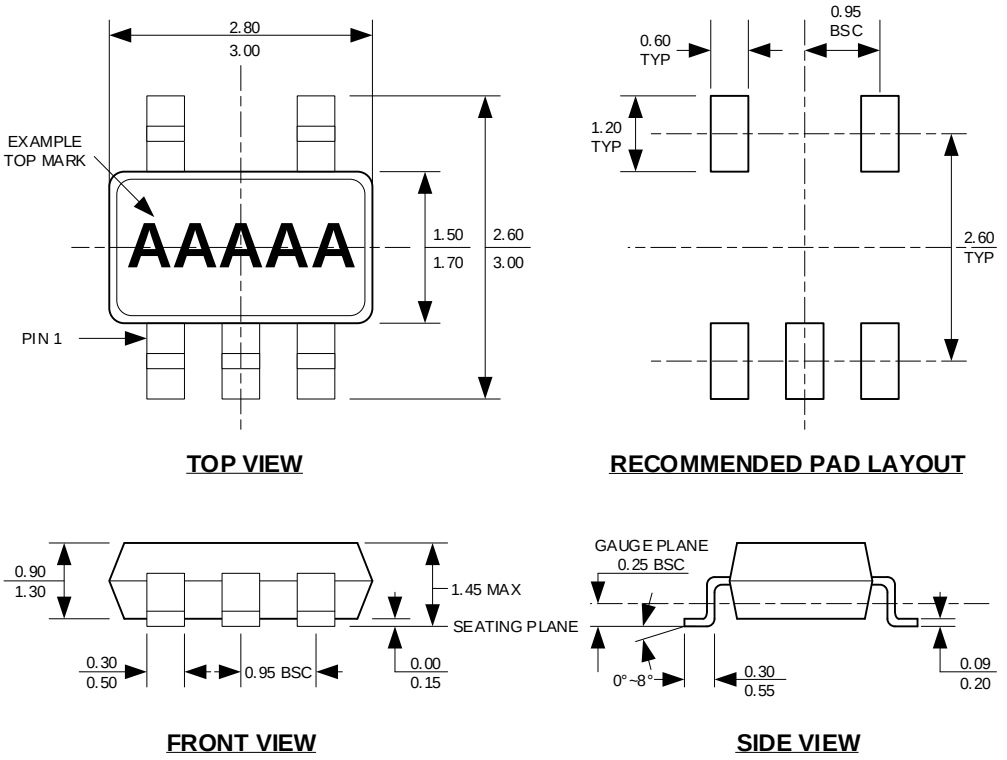
Ordering Device No.	Marking	Package	Packing	Quantity
ASP3420ZD-R	ADYLL	SOT23-5	Tape&Reel	3000/Reel

Top Marking:ADYLL(device code:AD,Y=year code,LL=lot number code)

PACKAGE	MARKING
SOT23-5	

Package Description

SOT23-5



NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

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