

General Features

- Low Gate Charge
- Advanced Trench Technology
- Provide Excellent RDS(ON)
- High Power and Current Handling Capability

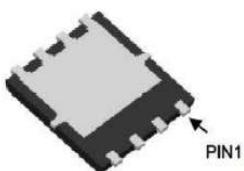
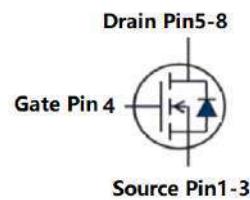
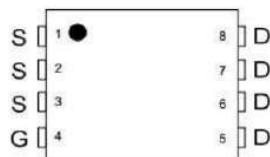
Application

- Load Switch
- PWM applications
- Power management

Product Summary



VDS	30	V
RDS(on),Typ.@ VGS=10 V	4.3	mΩ
ID	90	A


DFN5⁺6-8

N-Channel

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^B	I_D	90	A
$T_C = 100^\circ\text{C}$	I_D	40	
Pulsed Drain Current ^A	I_{DM}	360	A
Avalanche Current ^A	I_S	90	A
Single Pulse Avalanche Energy ^A $L = 0.3\text{mH}$	E_{AS}	135	mJ
Power Dissipation ^C	P_D	65	W
$T_C = 100^\circ\text{C}$	P_D	32	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	°C
Thermal Characteristics			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Case	Steady-State $R_{\Theta JC}$	2.3	°C/W
Maximum Junction-to-Ambient	Steady-State $R_{\Theta JA}$	62	

Electrical Characteristics($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	$T_J = 25^\circ\text{C}$	--	--	1
			$T_J = 125^\circ\text{C}$	--	--	25
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	--	--	± 100	nA
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.6	2.4	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	--	4.3	5.2	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 30\text{A}$	--	6.9	9.0	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 20\text{A}$	16	--	--	S
V_{SD}	Diode Forward Voltage	$I_S = 30\text{A}, V_{GS} = 0\text{V}$	--	--	1	V
I_S	Maximum Body-Diode Continuous Current ^B	--	--	--	90	A

DYNAMIC PARAMETERS

C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 15\text{V}, f = 1\text{MHz}$	--	2120	--	pF
C_{oss}	Output Capacitance		--	307	--	
C_{rss}	Reverse Transfer Capacitance		--	253	--	

SWITCHING PARAMETERS

Q_g	Total Gate Charge	$V_{GS} = 10\text{V}, V_{DS} = 15\text{V}, I_D = 30\text{A}$	--	40	--	nC
Q_{gs}	Gate Source Charge		--	5.4	--	
Q_{gd}	Gate Drain Charge		--	9.6	--	
$t_{D(on)}$	Turn-On Delay Time	$V_{GS} = 10\text{V}, V_{DS} = 15\text{V}, I_D = 20\text{A}, R_G = 3\Omega$	--	15	--	ns
t_r	Turn-On Rise Time		--	32	--	
$t_{D(off)}$	Turn-Off Delay Time		--	15	--	
t_f	Turn-Off Fall Time		--	12	--	
t_{rr}	Body Diode Reverse Recovery Time	$I_F = 30\text{A}, di/dt = 100\text{A}/\mu\text{s}$	--	23	--	ns
Q_{rr}	Body Diode Reverse Recovery Charge		--	48	--	nC

- A. Single pulse width limited by maximum junction temperature.
- B. The maximum current rating is package limited.
- C. The power dissipation P_D is based on $T_{J(\text{MAX})} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

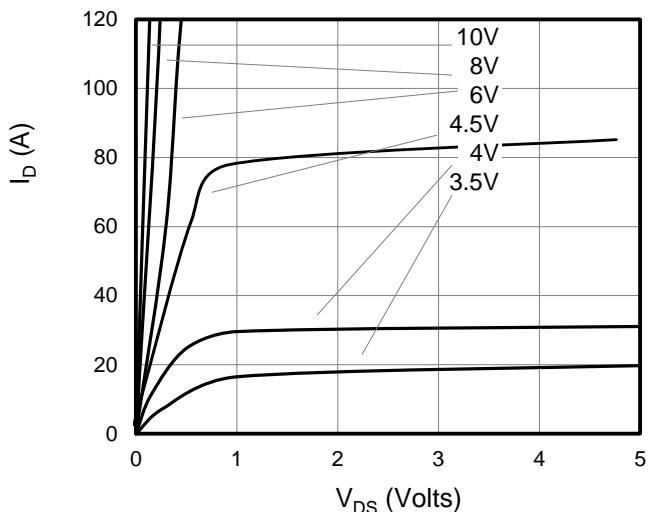


Figure 1: On-Region Characteristics

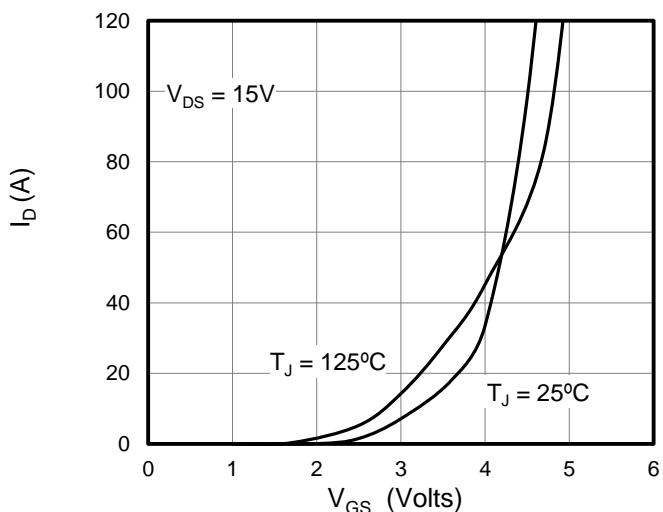


Figure 2: Transfer Characteristics

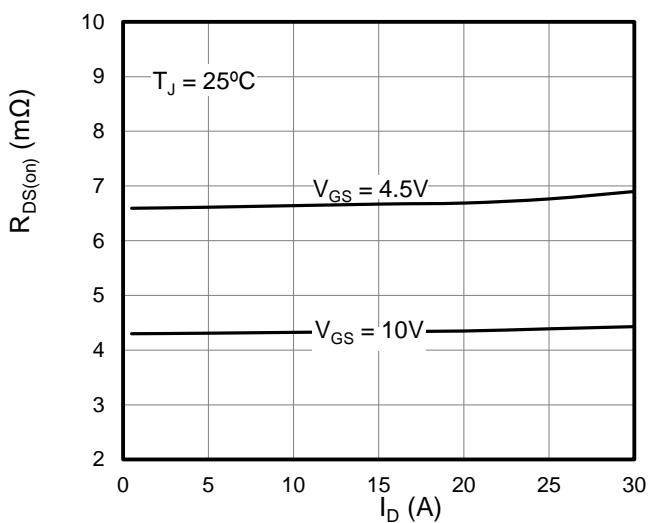


Figure 3: On-Resistance vs. Drain Current

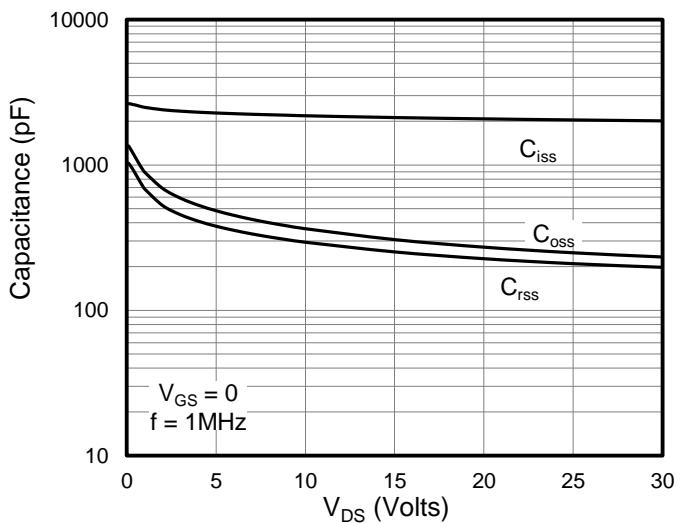


Figure 4: Capacitance Characteristics

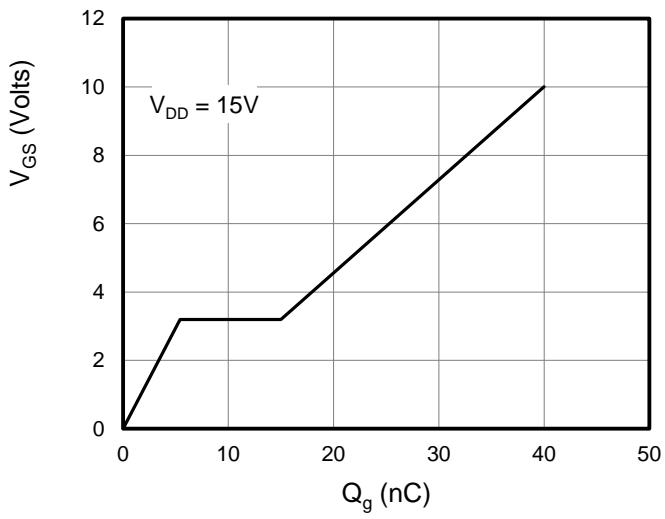


Figure 5: Gate Charge Characteristics

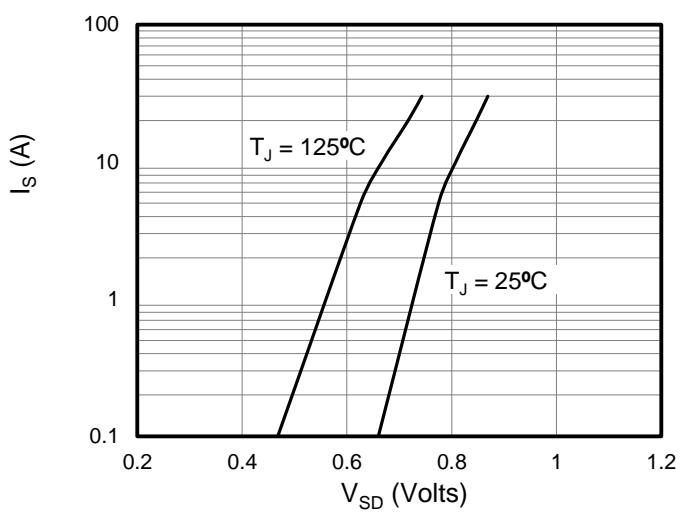


Figure 6: Body Diode Forward Voltage

Typical Characteristics $T_J = 25^{\circ}\text{C}$, unless otherwise noted

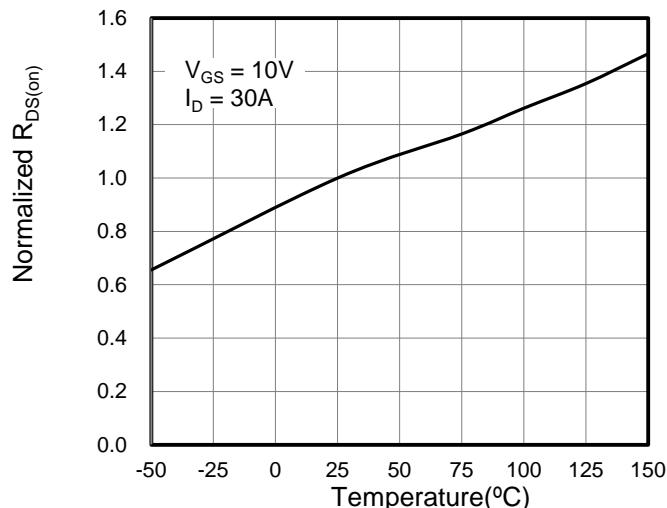


Figure 7: On-Resistance vs. Junction Temperature

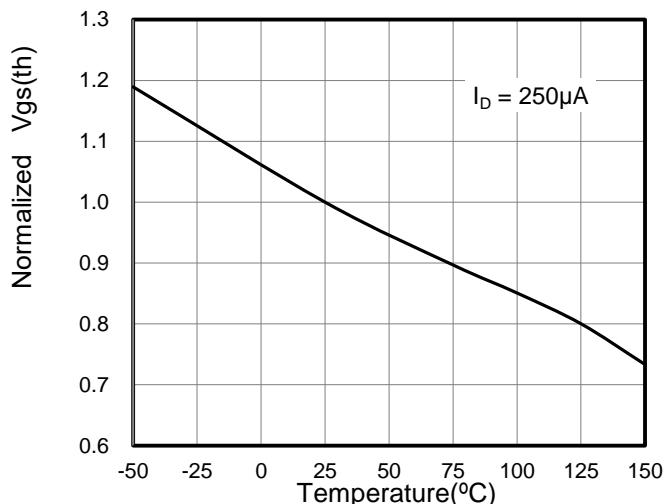


Figure 8: Vgs(th) vs. Junction Temperature

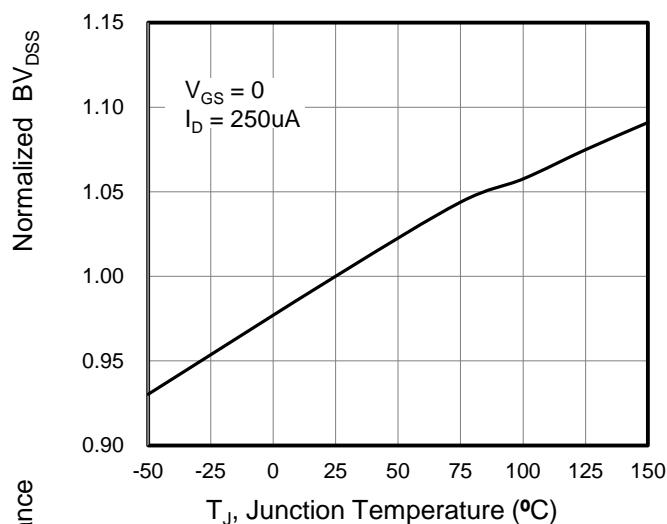


Figure 9: BV_{DSS} vs. Junction Temperature

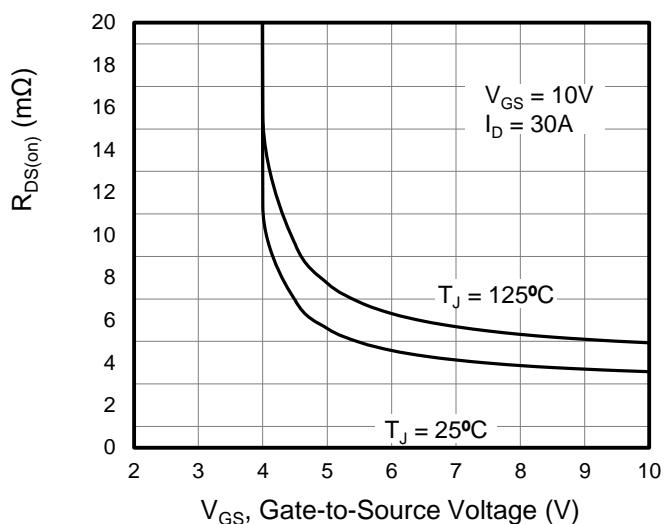


Figure 10: On-Resistance vs. Gate-Source Voltage

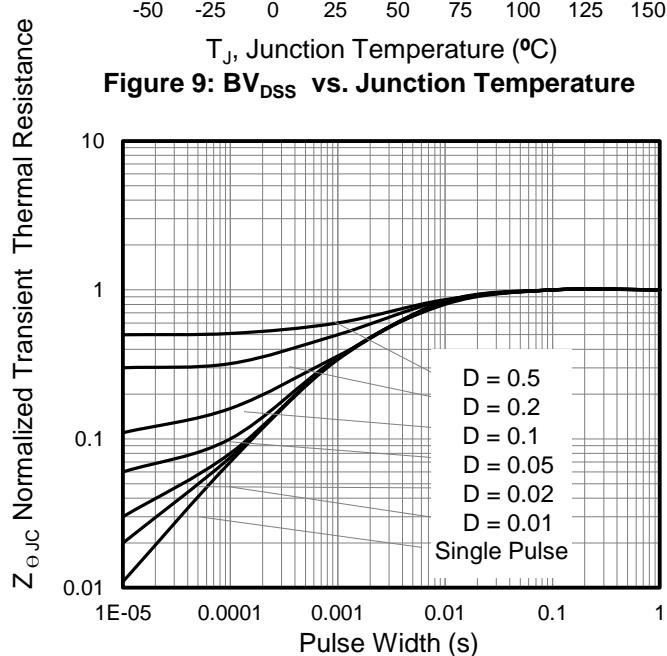


Figure 11: Normalized Transient Thermal Resistance

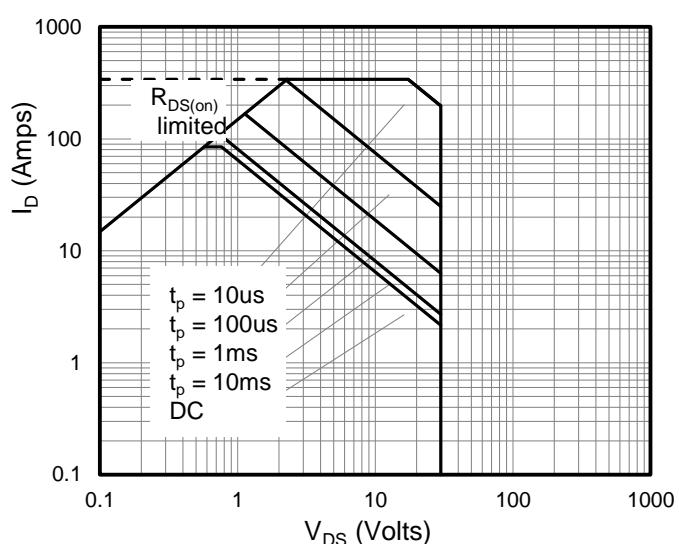


Figure 12: Safe Operating Area

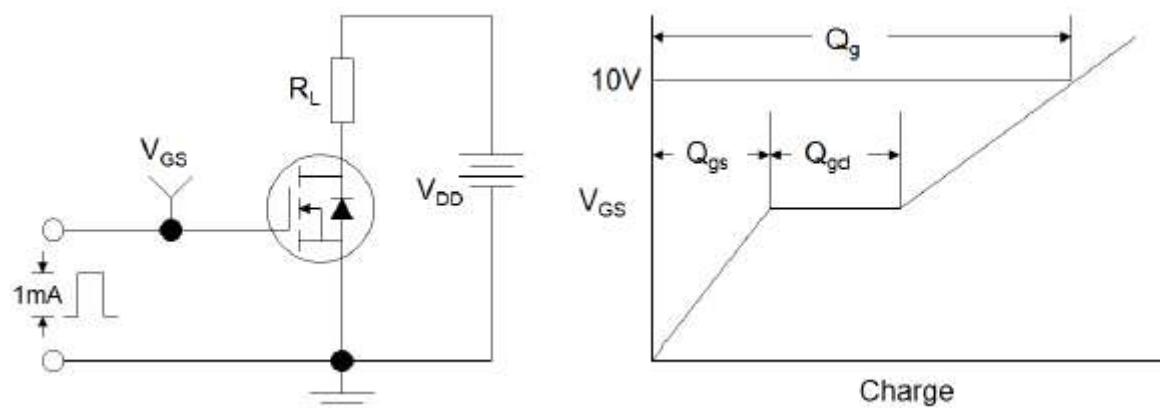


Figure1:Gate Charge Test Circuit & Waveform

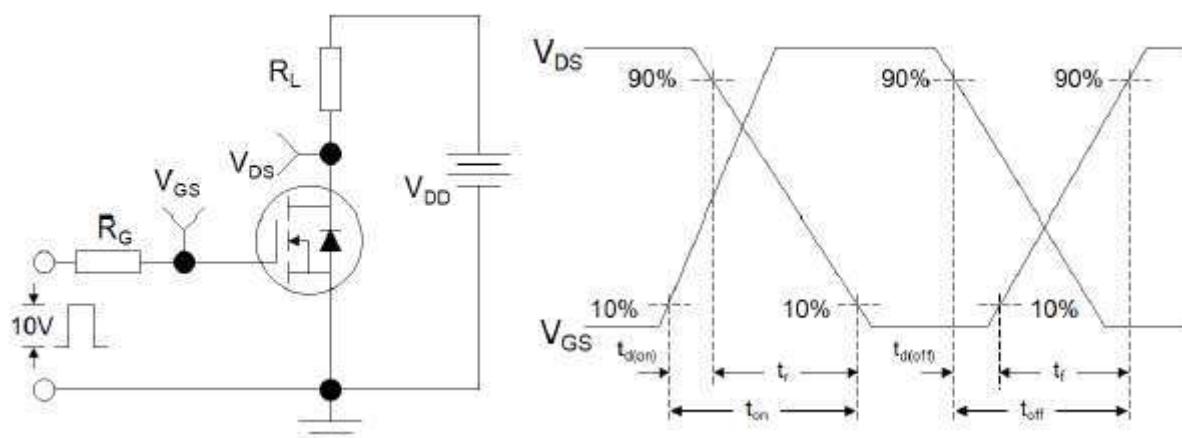


Figure 2: Resistive Switching Test Circuit & Waveforms

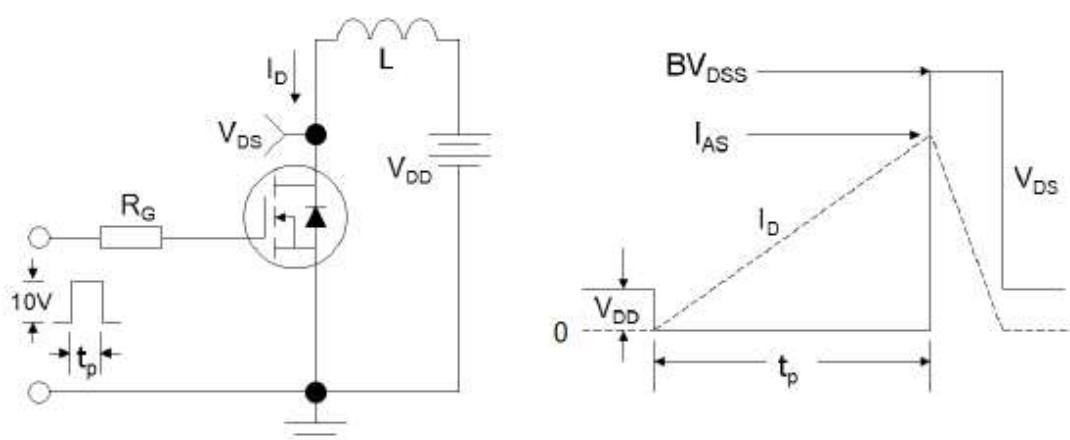


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

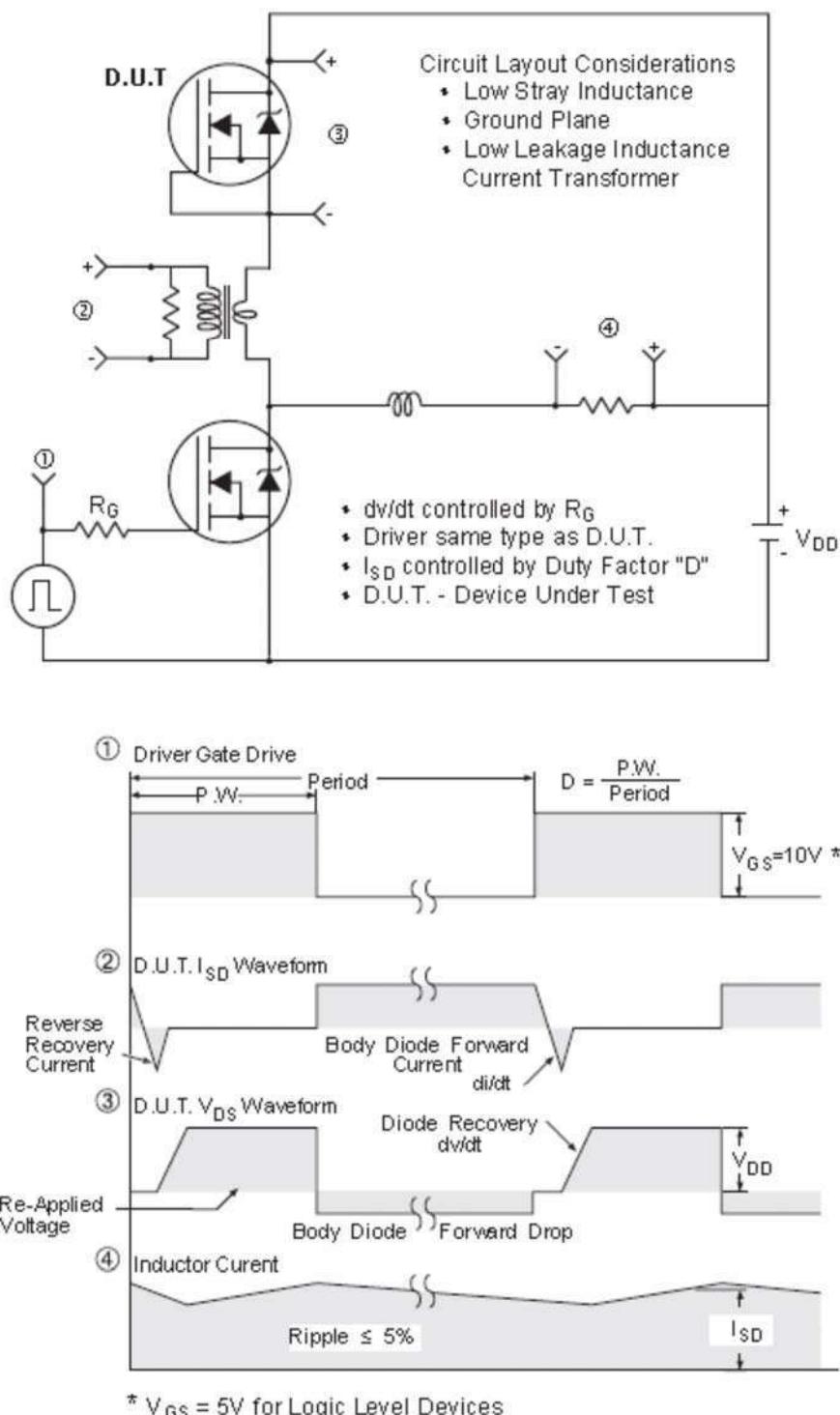
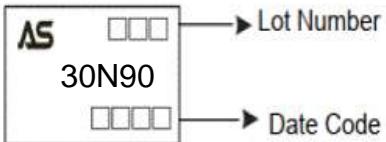
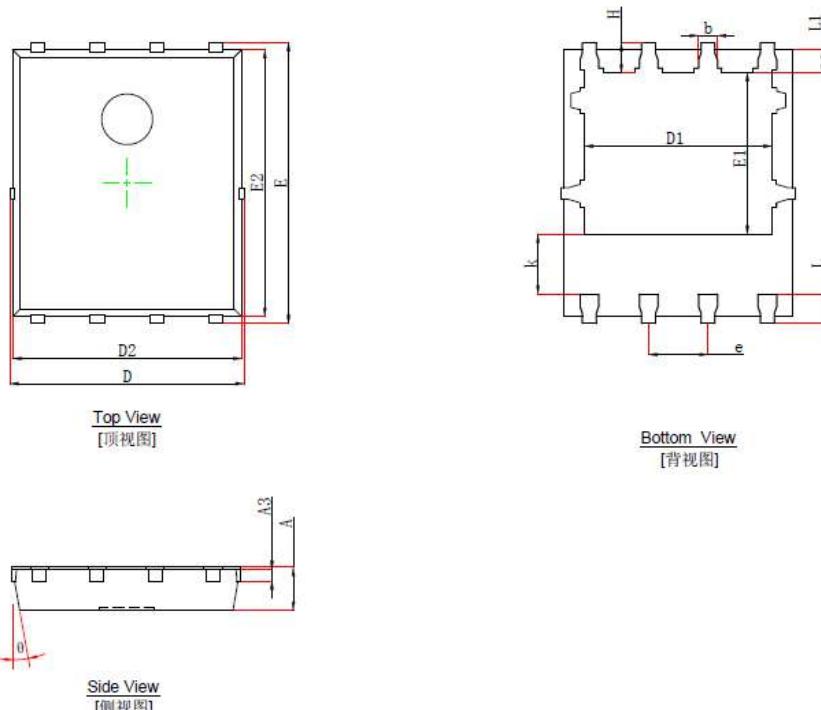


Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM30N90Q-R	30N90	DFN5*6-8	Tape&Reel	4000/Reel

PACKAGE	MARKING
DFN5*6-8	

DFN5*6- 8 PACKAGE IN FORMATION


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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