

#### **General Features**

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E<sub>AS</sub>
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

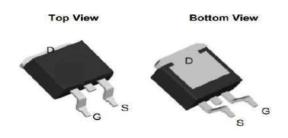
## **Application**

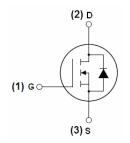
- Power switching application
- LED backlighting
- Uninterruptible power supply





BVDSS	60	V
RDS(on),Typ.@VGS=10V	6.4	mΩ
ID	80	Α





TO-263

Absolute Maximum Ratings (T<sub>c</sub>=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	60	V	
Gate-Source Voltage	Vgs	±20	V	
Drain Current-Continuous	I <sub>D</sub>	80	Α	
Drain Current-Continuous(T <sub>C</sub> =100°C)	I <sub>D</sub> (100℃)	56	А	
Pulsed Drain Current	I <sub>DM</sub>	250	А	
Maximum Power Dissipation	P <sub>D</sub>	85	W	
Debating factor		0.57	W/℃	
Single pulse avalanche energy (Note 5)	E <sub>AS</sub>	125	mJ	
Operating Junction and Storage Temperature Range	$T_{J}, T_{STG}$	-55 To 175	$^{\circ}$	

### **Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient (Note 2)	R <sub>0JA</sub>	62	°C/W
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{ heta JC}$	0.76	°C/W



# Electrical Characteristics (T<sub>C</sub>=25 ℃ unless otherwise noted)

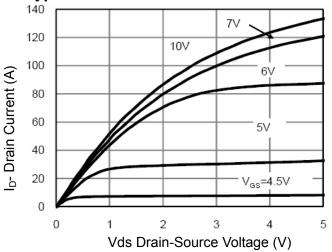
Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	•		•			
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =60V,V <sub>GS</sub> =0V	-	-	1	μΑ
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics (Note 3)			•			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_{D}=250\mu A$	2	2.8	4	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A	-	6.4	10	mΩ
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =5V,I <sub>D</sub> =30A	30	-	-	S
Dynamic Characteristics (Note4)	<u> </u>		•			
Input Capacitance	C <sub>lss</sub>	\/ OF\/\/ O\/	-	2498	-	PF
Output Capacitance	C <sub>oss</sub>	$V_{DS}$ =25V, $V_{GS}$ =0V,	-	185	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>	F=1.0MHz	-	80	-	PF
Switching Characteristics (Note 4)	<u> </u>		•			
Turn-on Delay Time	t <sub>d(on)</sub>		-	12	-	nS
Turn-on Rise Time	t <sub>r</sub>	$V_{DD}$ =30V, $I_D$ =2A, $R_L$ =1 $\Omega$	-	5.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$	$V_{GS}$ =10 $V$ , $R_{GEN}$ =3 $\Omega$	-	38	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	27	-	nS
Total Gate Charge	Qg	\/ 00\/\ 00\	-	36	-	nC
Gate-Source Charge	$Q_{gs}$	V <sub>DS</sub> =30V,I <sub>D</sub> =30A,	-	9.9	-	nC
Gate-Drain Charge	$Q_{gd}$	V <sub>GS</sub> =10V	-	6.6	-	nC
Drain-Source Diode Characteristics			II			
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =20A	-	-	1.4	V
Diode Forward Current (Note 2)	Is		-	-	80	Α
Reverse Recovery Time	t <sub>rr</sub>	TJ = 25°C, IF =30A	-	35		nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs <sup>(Note3)</sup>	-	47		nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD				y LS+LD)

#### Notes:

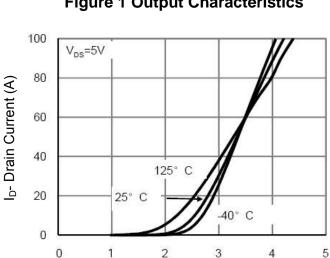
- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to production
- **5.** E<sub>AS</sub> condition: Tj=25  $^{\circ}$ C,V<sub>DD</sub>=30V,V<sub>G</sub>=10V,L=0.5mH,Rg=25 $\Omega$



## Typical Electrical and Thermal Characteristics (Curves)



**Figure 1 Output Characteristics** 



Vgs Gate-Source Voltage (V) **Figure 2 Transfer Characteristics** 

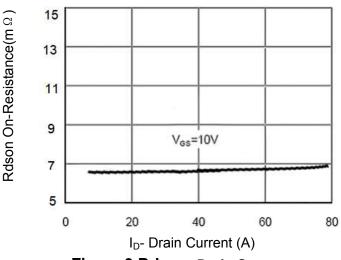


Figure 3 Rdson- Drain Current

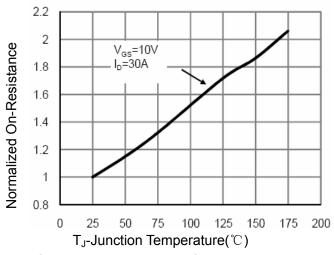


Figure 4 Rdson-JunctionTemperature

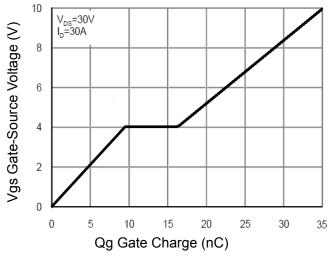


Figure 5 Gate Charge

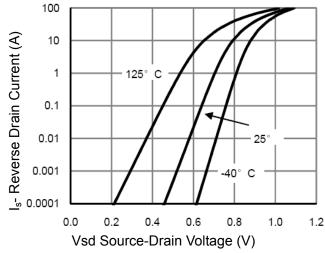
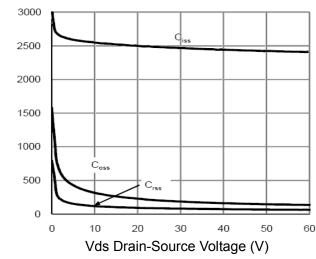


Figure 6 Source- Drain Diode Forward



C Capacitance (pF)

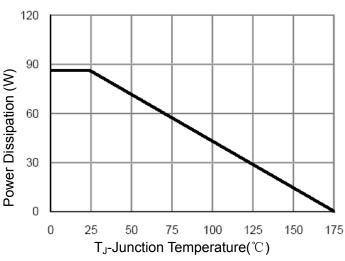


Figure 7 Capacitance vs Vds



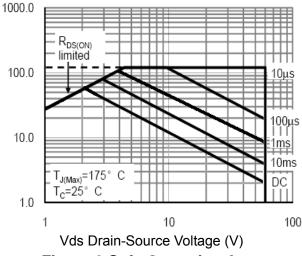


Figure 8 Safe Operation Area

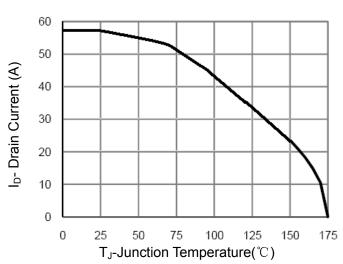


Figure 10 ID Current- JunctionTemperature

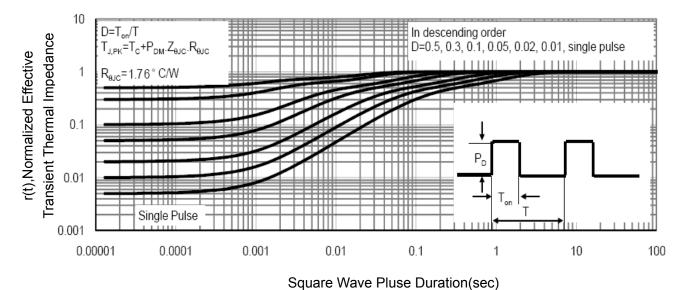


Figure 11 Normalized Maximum Transient Thermal Impedance



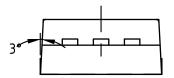
# **Ordering and Marking Information**

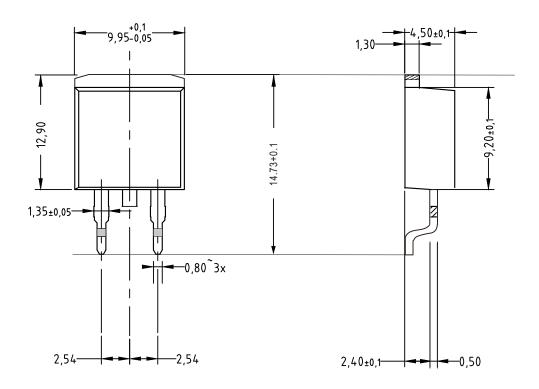
Ordering Device No.	Marking	Package	Packing	Quantity
ASDM60N80G-R	60N80	TO-263	Reel&Tape	800/Reel

MARKING			
Lot Number 60N80 □□□□□ ➤ Date Code			



# TO-263









60V N-Channel MOSFET

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