18V, 6A Synchronous Step-Down Converter

Overview

The ASP206AS is a fully integrated easy-to-use synchronous step-down converter, which integrated low on resistance high-side and low-side power MOSFETs. The ASP206AS can deliver 6A of output current efficiently with constant on time (COT) control for fast loop response.

The ASP206AS achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

The ASP206AS has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, output over voltage protection, FB open protection and thermal shutdown in case of excessive power dissipation. The ASP206AS is available in a space-saving ESOP-8 package.

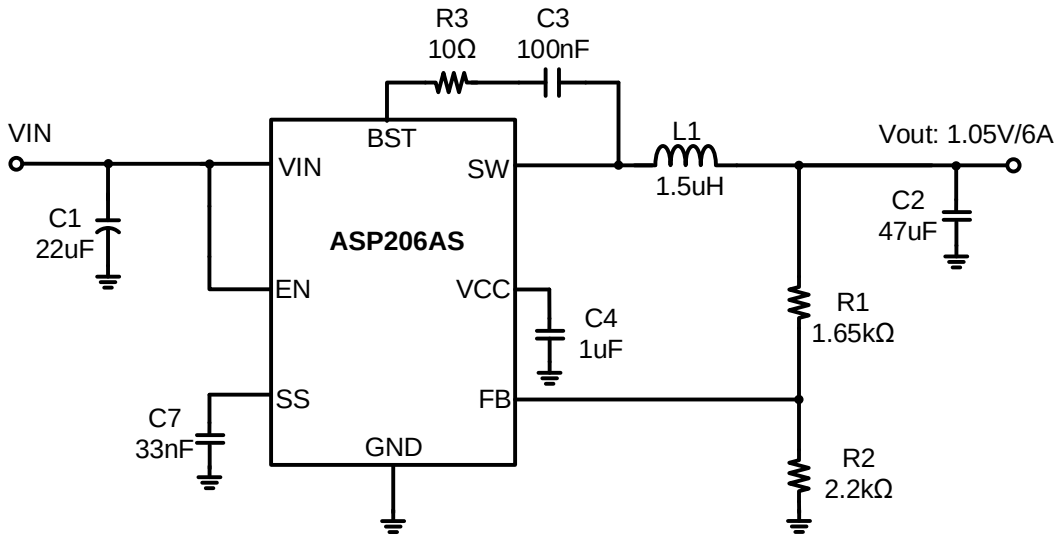
Features

- 4.5V to 18V Input Voltage range
- 36.5mΩ/17.5mΩ Power MOSFET
- 6A Continuous Output Current
- 305μA Low Quiescent Current
- Constant On Time Control for Fast Loop Response
- Soft Start Time Programmable
- Support Up to 99.5% Large Range Duty Cycle
- Output Discharge
- Output Voltage Adjustable from 0.6V
- Support Pre-Biased Output Startup
- Full Protection, Over Current Protection and Hiccup, Output Over Voltage Protection, Over Temperature Protection
- Available in an ESOP-8 Package

Applications

- General Purpose Point-of-Load (POL)
- 12V Distribution Power Systems
- Television

• Typical Application

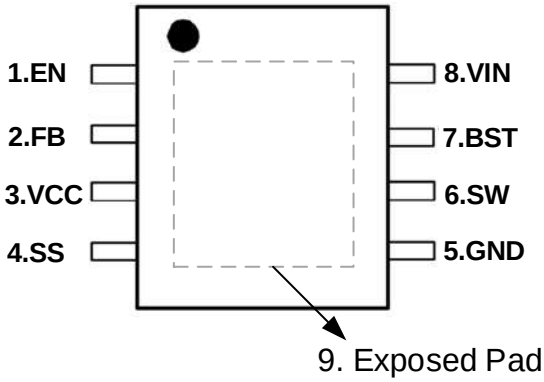


Order Information

Device No.	Package	Quantity
ASP206ASW-R	ESOP-8	4000pcs/Reel

Note: "S" stands for Soft start Funtion.
Note: "W" stands for package. "W": ESOP-8.
Note: "R" stands for Packing, Tape&Reel.

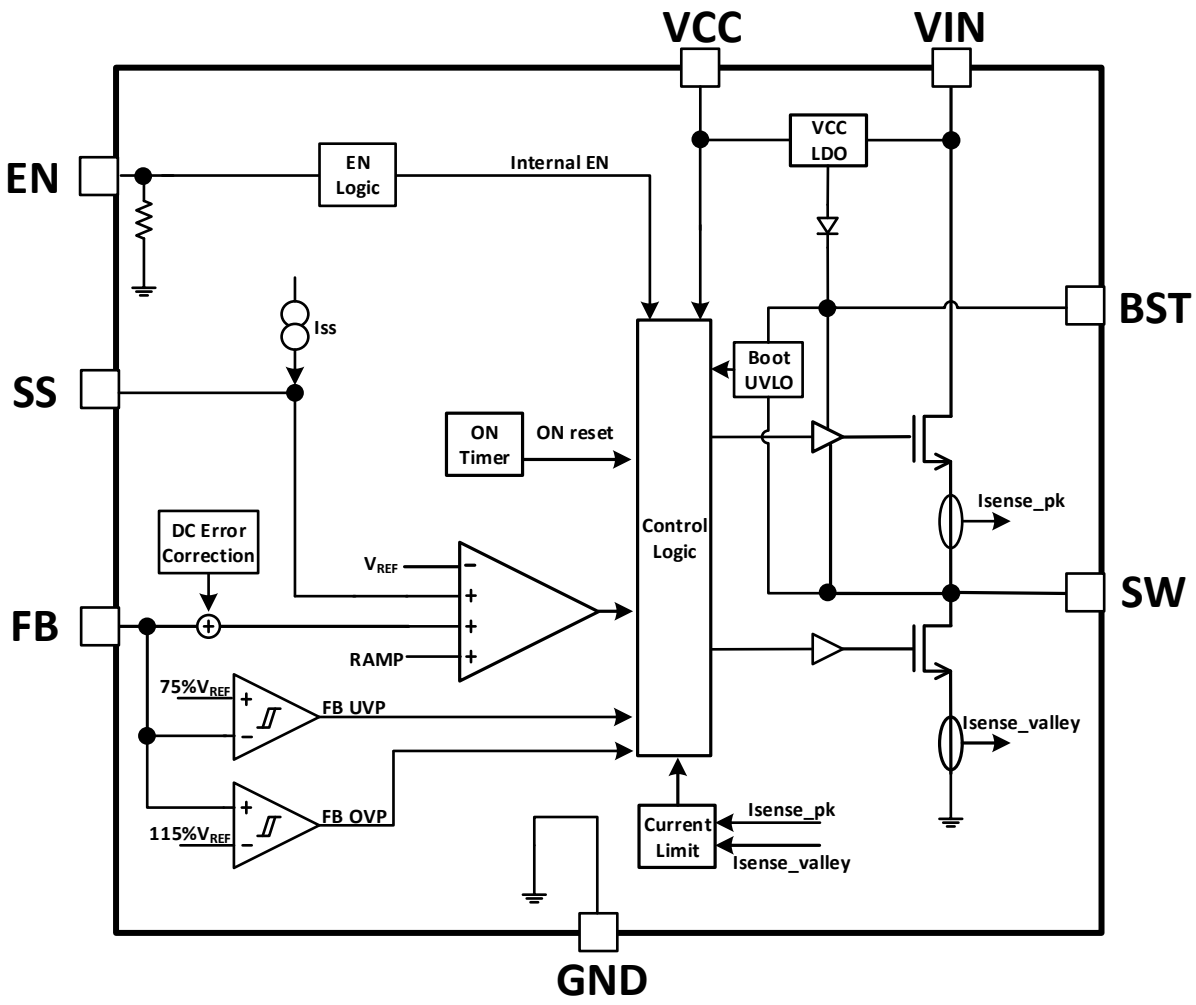
Pin Diagram



Pin Description

Pin No.	Symbol	Pin Description
1	EN	**Enable.** High = on, low = off. Can be tied to VIN by a directly. Precision enable input allows adjustable UVLO by external resistor divider.
2	FB	**Feedback.** Connect a resistor divider to set the output voltage.
3	VCC	**Internal 5V LDO output.** Decouple VCC with a 1μF capacitor Place capacitor close to VCC and GND.
4	SS	**Soft start pin.** Connect a capacitor from SS to GND to set the soft start time. Do not float this pin.
5	GND	**Ground of the chip.** Connect to the ground of the system.
6	SW	**Switching node of power stage.** Connect to power inductor.
7	BST	**Bootstrap.** Connect a high quality capacitor between this pin and SW pin.
8	VIN	**Input voltage supply.** Connect a capacitor between VIN pin and GND pin. Use wide PCB traces to make the connection.
9	EP	**Exposed Pad.** Connect exposed pad to the PCB GND plane to achieve good thermal performance.

Block Diagram



Absolute Maximum Ratings (1)

T_A=25°C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
V_{IN}	VIN to GND	-0.3~20	V
V_{EN}	EN to GND	-0.3~20	V
V_{SW}	SW to GND	-0.7 ~ VIN + 0.7	V
V_{BST}-V_{SW}	BST to SW	-0.3~6	V
All Other Pins		-0.3~6	V
T_{STG}	Storage temperature	-55 to 150	°C
T_J	Junction temperature	-40 to 150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
V_{IN}	VIN to GND	4.5~18	V
V_{OUT}	VOUT to GND	0.6~13	V
I_{OUT}	Max Continuous Output Current	6	A

Thermal Resistance (2)

Symbol	Definition	Ratings	Unit
$R_{\theta JC(TOP)}$	Junction to case (top) thermal resistance	52	°C/W
$R_{\theta JC(BOT)}$	Junction to case (bottom) thermal resistance	2.3	°C/W
$R_{\theta JA}$	Junction to ambient thermal resistance	48	°C/W

Note 2: Measured on JESD51-7, 4-Layer PCB, and the PCB has no copper for thermal dissipation. Normal PCB with copper thermal resistance will be smaller.

ESD Rating

Symbol	Definition	Ratings	Unit
HBM	Human body model	± 2000	V
CDM	Changed device model	± 500	V

Electrical Characteristics

V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input UVLO and Quiescent Current						
VCC_{UVR}	VCC rising threshold			3.65		V
VCC_{UVF}	VCC falling threshold			3.15		V
VCC_{UV_hys}	VCC UVLO hysteresis			0.5		V
I_S	Shutdown supply current	V_{IN}=18V		1	3	μA
I_Q	Quiescent supply current	No load, V_{FB} = 0.65V, no switching		305		μA
EN						
V_{EN1_R}	Enable rising threshold	Low to high		1.25		V
V_{EN_F}	Enable falling threshold	High to low		1.05		V
V_{EN_Hys}	Enable Threshold Hysteresis			0.2		V
R_{EN}	Enable input resistor.			1500		kΩ
VCC REGULATOR						
V_{CC}	VCC regulator	V_{IN} > 5.2V		5		V
I_{VCC}	VCC Current Limit	V_{CC} drops to 4.5V	20			mA
Buck Feedback Voltage and SS						
V_{FB}	Feedback voltage		594	600	606	mV
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
Buck High Side and Low Side MOSFETs						
R_{ON_HS}	High-side MOSFET on-resistance	V_{BST} - V_{SW} = 5V		36.5		mΩ
R_{ON_LS}	Low-side MOSFET on-resistance	V_{IN} = 12V		17.5		mΩ
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V		0.1		μA
LKG_{LS}	Low-side leakage	V_{EN} = 0V, V_{SW} = 12V		12		μA
Output Discharge Resistor						
$R_{DISCHARGE}$				190		Ω

Electrical Characteristics

V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Buck Current Limit						
I_{LIM_LS}	Low-side Valley Current limit			6.5		A
I_{LIM_HS}	High-side Peak Current limit			7.8		A
I_{NOC}	Negative Current Limit			3.5		A
Buck Output OVP and UVP						
$V_{OVP\_rising\_th}$	Output OVP rising threshold			115%		V_{FB}
$V_{OVP\_falling\_th}$	Output OVP falling threshold			105%		V_{FB}
$V_{UVP\_falling\_th}$	UVP threshold falling threshold			75%		V_{FB}
$V_{UVP\_rising\_th}$	UVP threshold rising threshold			85%		V_{FB}
Soft-start						
I_{SS_charge}	SS charge current			10		μA
$I_{SS\_discharge}$	SS discharge current			2.5		mA
Switching Frequency						
F_{SW}	Oscillator frequency			600		kHz
T_{ON_MIN}	Minimum switch on time (3)			60		ns
T_{OFF_MIN}	Minimum switch off time (3)			150		ns
D_{MAX}	Maximum duty cycle(3)			99.5		%
Thermal Protection						
T_{OTP_R}	Thermal shutdown (3)			160		°C
T_{OTP_F}	Thermal shutdown hysteresis (3)			140		°C
T_{OTP_Hys}	OTP hysteresis(3)			20		°C

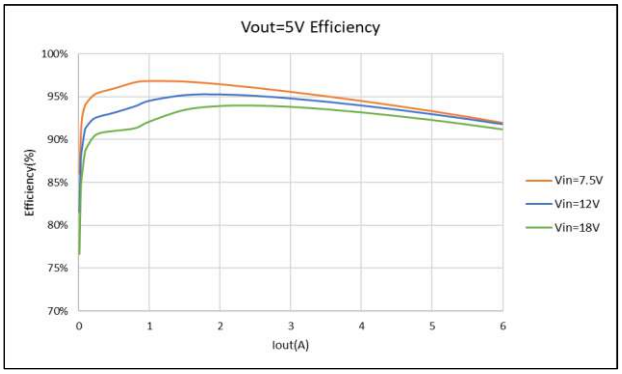
Note 3: Guaranteed by design and engineering sample characterization.

Typical Characteristic

V_{IN} = 12V, V_{OUT} = 5V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 3.3μH, T_A = +25°C, unless otherwise noted.

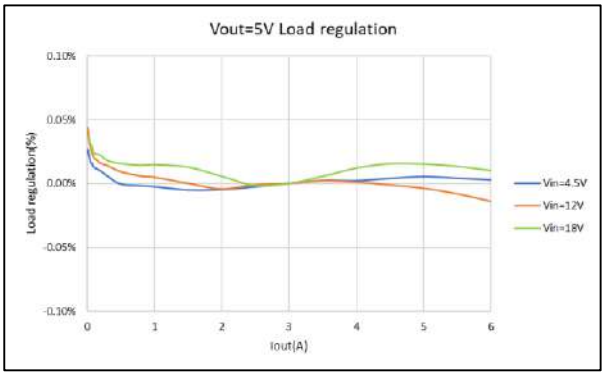
Efficiency vs. Load Current

F_{SW}=600kHz, Rbst=10Ω



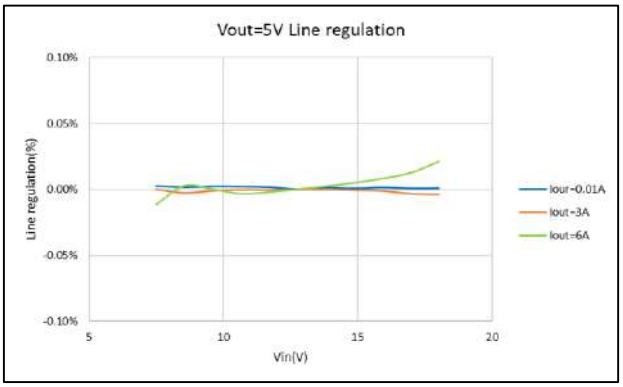
Load Regulation

F_{SW}=600kHz



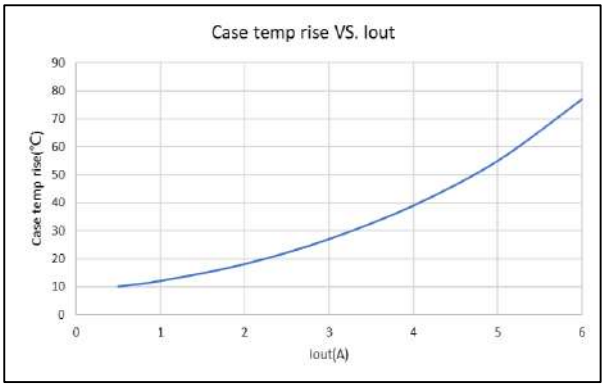
Line Regulation

F_{SW}=600kHz



Thermal Rise

F_{SW}=600kHz , no air flow

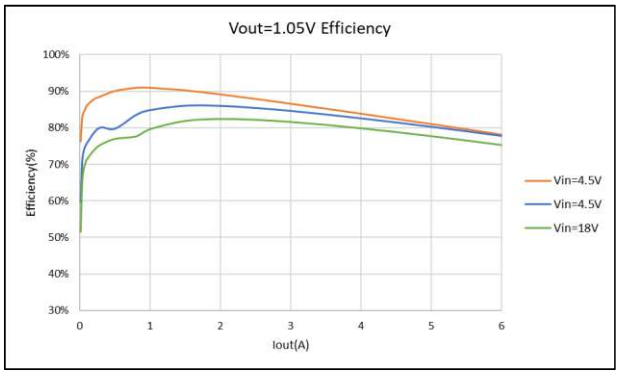


Typical Characteristic*(continued)*

V_{IN} = 12V, V_{OUT} = 1.05V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 1.5μH, T_A = +25°C, unless otherwise noted.

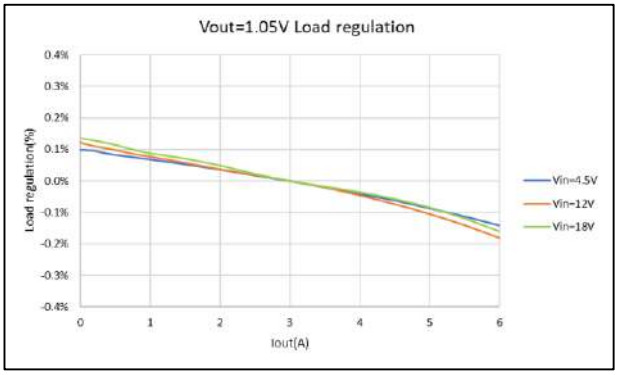
Efficiency vs. Load Current

F_{SW}=600kHz, Rbst=10Ω



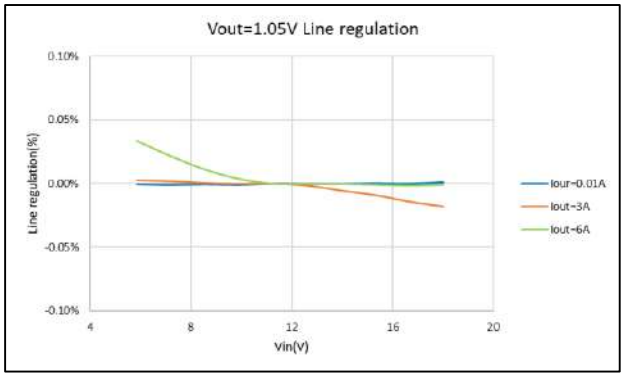
Load Regulation

F_{SW}=600kHz



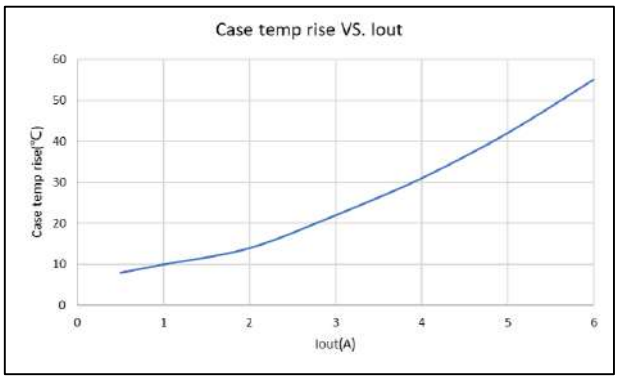
Line Regulation

F_{SW}=600kHz

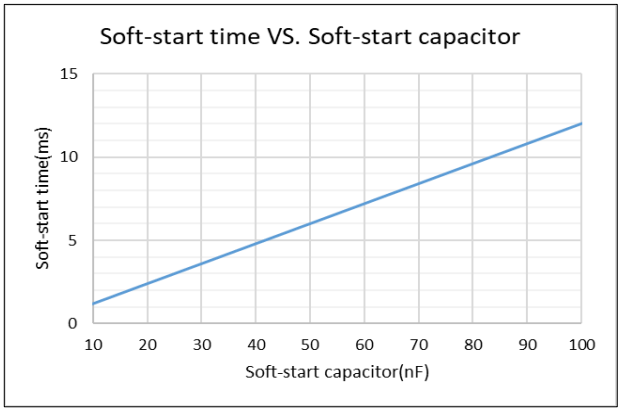


Thermal Rise

F_{SW}=600kHz , no air flow



Soft-start time VS. Soft-start capacitor

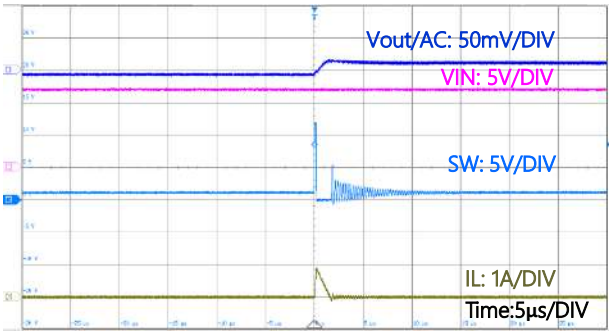


Typical Performance Characteristic

V_{IN} = 12V, V_{OUT} = 1.05V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 1.5μH, C_{SS}=33nF, and T_A = +25°C, unless otherwise noted.

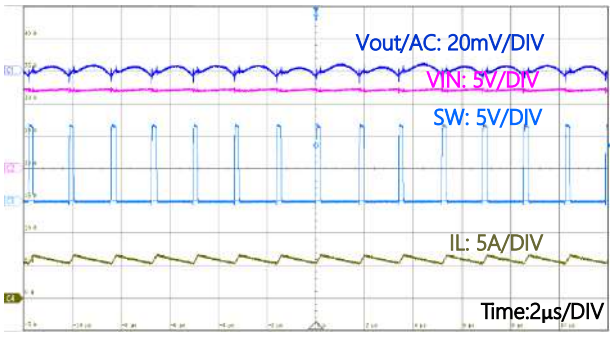
Output Voltage Ripple

I_{OUT}=0A



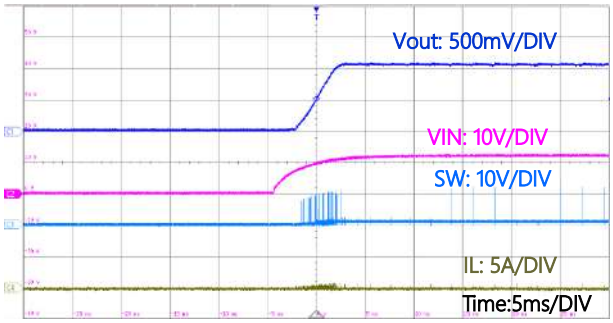
Output Voltage Ripple

I_{OUT}=6A



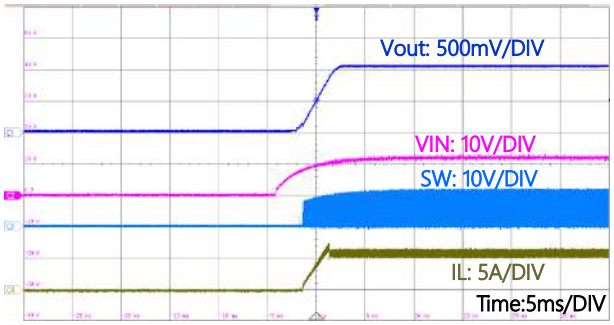
Start-Up through V_{IN}

I_{OUT}=0A



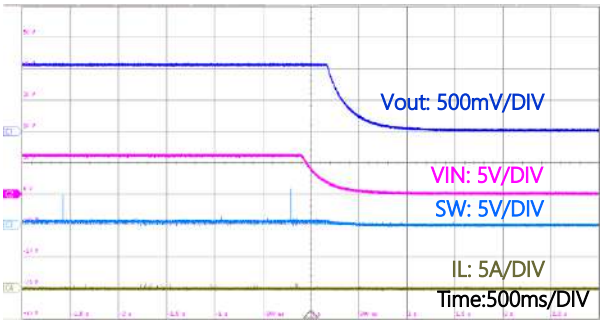
Start-Up through V_{IN}

I_{OUT}=6A



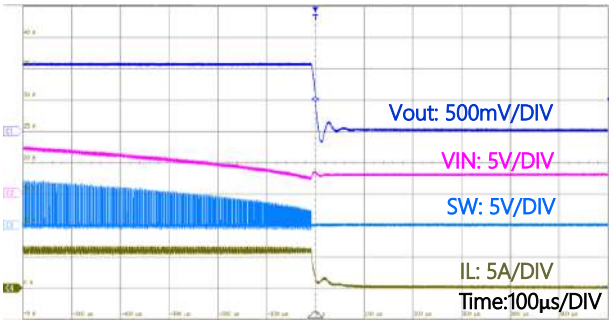
Shut-Down through V_{IN}

I_{OUT}=0A



Shut-Down through V_{IN}

I_{OUT}=6A

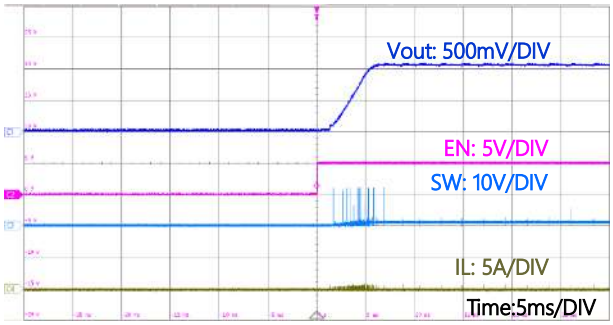


Typical Performance Characteristic*(continued)*

V_{IN} = 12V, V_{OUT} = 1.05V, C_{IN} = 22μF, C_{OUT} = 44μF, L1 = 1.5μH, C_{SS}=33nF, and T_A = +25°C, unless otherwise noted.

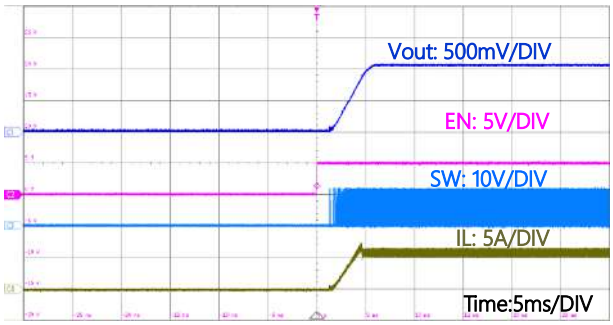
Start-Up through EN

I_{OUT}=0A



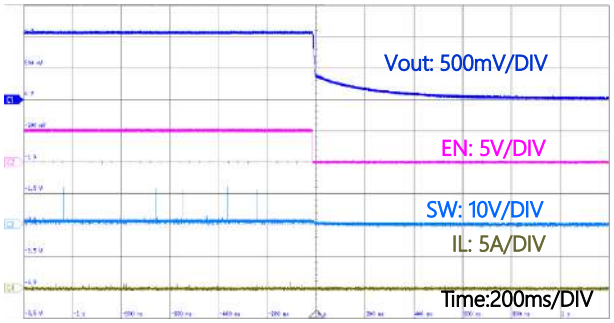
Start-Up through EN

I_{OUT}=6A



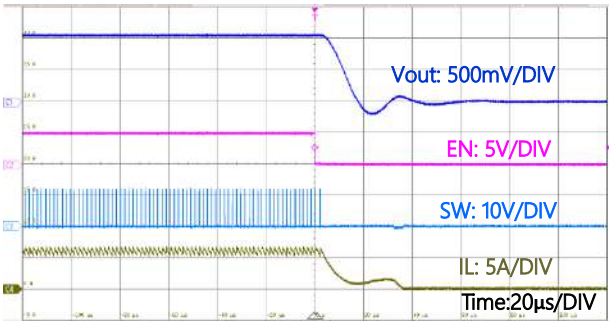
Shut-Down through EN

I_{OUT}=0A



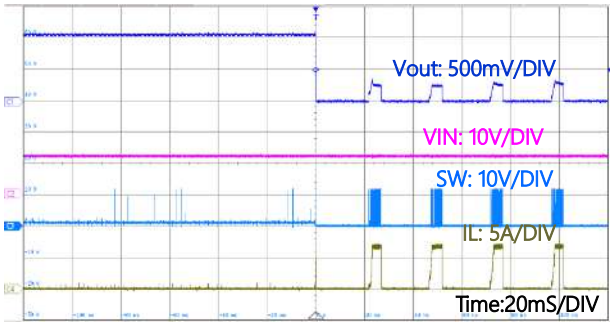
Shut-Down through EN

I_{OUT}=6A



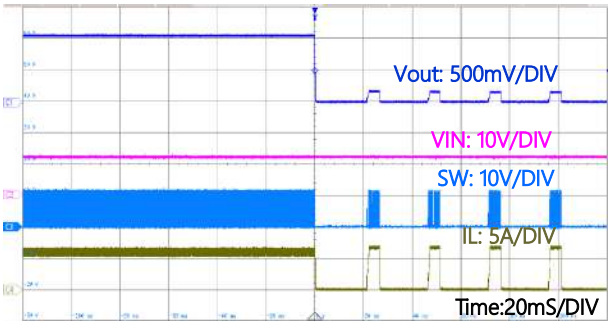
Short-Circuit Entry

I_{OUT}=0A



Short-Circuit Entry

I_{OUT}=6A



Typical Performance Characteristic*(continued)*

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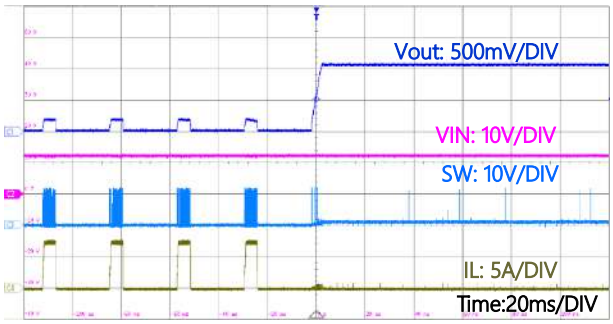
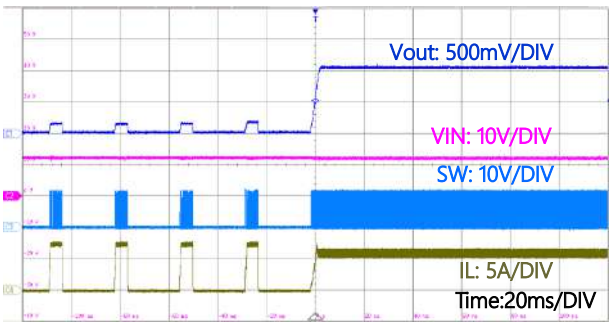
Short-Circuit Recovery

I_{OUT}=0A

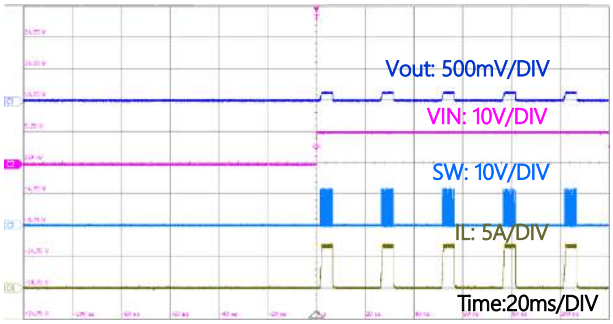


Short-Circuit Recovery

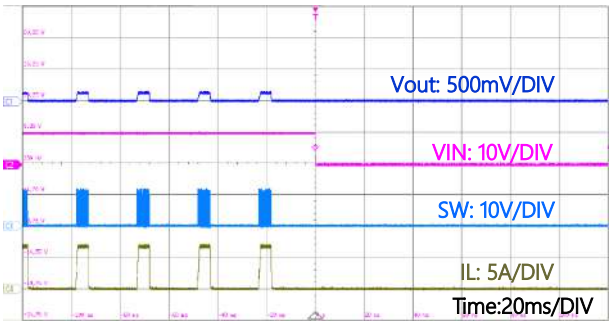
I_{OUT}=6A



Short-circuit EN power on

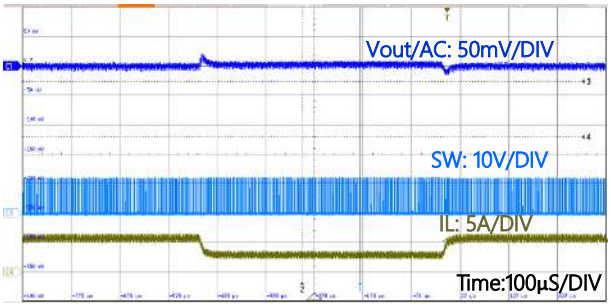


Short-circuit EN power off



Load Transient

I_{OUT} = 3A to 6A, slew rate=3A/µs setting by E-load



Function Descriptions

COT control loop operation

The ASP206AS is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range. After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS- FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS- FET off and HS-FET on period.

Light Load operation(PFM)

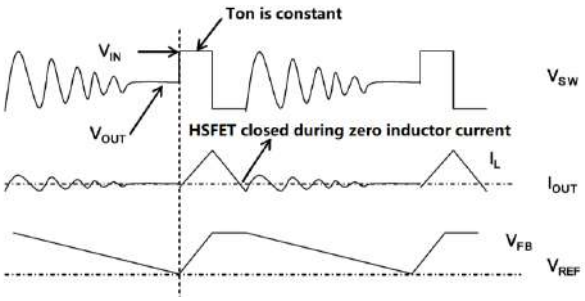


Figure 1: Light Load Operation

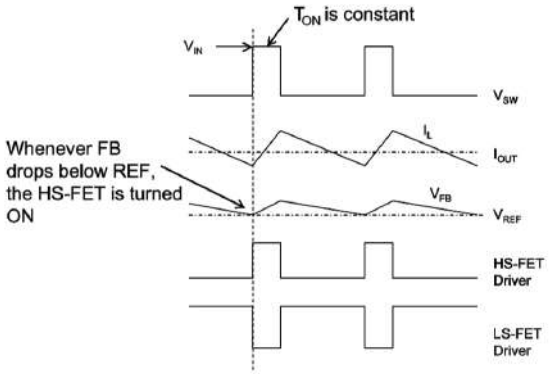


Figure 2: Heavy Load Operation

In light load condition, V_{FB} can't reach V_{REF} while the inductor current is approaching zero, a current modulator takes over control of the LS-FET and limits the inductor current around zero, and the LS-FET driver enters hi-z state since that time, the output drop speed is very slow, thus the ASP206AS reduces the switching frequency naturally, and high efficiency is achieved. As a trade-off, PFM mode suffers larger V_{OUT} ripple.

Heavy Load operation(CCM)

With the load current increasing, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly.

The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT\_Critical} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{sw} \times V_{IN}} \quad (1)$$

The device enters CCM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Enable (EN) Control

The ASP206AS has a dedicated enable control pin with positive logic. Drive EN pin voltage higher than 1.25V(typical) to turn on the regulator, and drive EN pin voltage lower than 1.05V(typical) to turn it off. By using the two external resistor dividers, it is easy to optimize the start and stop voltage of the system via EN pin:

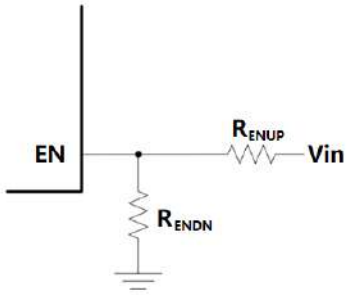


Figure 3: Enable network

Start voltage setting:

$$V_{START} = 1.25 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 1.05 \times \frac{R_{ENUP} + R_{ENDN}}{R_{ENDN}} \quad (3)$$

Tie EN pin to VIN directly to set IC automatically start-up.

VCC Under-Voltage Lockout (UVLO)

VCC Under-voltage lockout (UVLO) protects the chip from operating at an insufficient VCC voltage. The ASP206AS VCC UVLO comparator monitors the VCC voltage. The VCC UVLO rising threshold is about 3.65V, while its falling threshold is consistently 3.15V.

Soft Start (SS)

Adjust the soft-start time by connecting a capacitor from SS pin to GND. When the soft-start begins, an internal 10μA current source charges the external capacitor. During soft-start, the soft-start capacitor connects to the non-inverting input of the error amplifier. The soft-start period continues until the voltage on the soft-start capacitor exceeds the 1.2V. Then the non-inverting amplifier uses the reference voltage takes as the input. Please refer below calculation to set C_{SS}.

$$T_{SS}(ms) = \frac{1.2V \times C_{SS}(nF)}{10\mu A} \quad (4)$$

Pre-Bias Start-Up

The ASP206AS is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

Output Over-Voltage Protection(OVP)/Under-Voltage Protection(UVP)

The ASP206AS monitors a resistor-divided V_{FB} to detect over or under-voltage. When V_{FB} becomes higher than 115% of the target voltage, the over-voltage protection (OVP) comparator output goes to high, and the circuit will turn on LSFET to discharge the output. LSFET will be turned off until the negative current limit is triggered then LSFET will remain off for 5us to turn on again. IC will repeat above process until the output OVP condition is removed.

When V_{FB} drops below 75% of V_{REF}, the UVP comparator output goes to high, and the ASP206AS enters the hiccup protection.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The ASP206AS has both valley current-limit control and peak current limit control. During LS-FET on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the LS-FET limit comparator. The device enters overcurrent protection (OCP) mode, and the HS-FET waits until the valley current limit disappears before turning on again. During the HS-FET on period, the inductor current is compared with the peak current-limit. If the peak current limit is triggered, the HS-FET on pulse will be terminated immediately. The output voltage drops until V_{FB} is below the UVP threshold. Once FB UVP is triggered, the ASP206AS enters hiccup mode to restart the part periodically.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation level. OCP is a non-latch protection.

Large Duty Cycle Operation

When ASP206AS will automatically extend the frequency to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when $T_{OFF-MIN}$ time is reached. The ASP206AS can support up to 99.5% maximum duty cycle. Large duty cycle operation is disabled when OCP is triggered.

Thermal Shutdown

Thermal shutdown is employed in the ASP206AS. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off. This is a non-latched protection. There is a hysteresis of about 20°C. Once the junction temperature drops to about 140°C, a soft start is initiated.

Output Discharge

The ASP206AS has active output discharge path, when EN off signal is coming, a 190Ω resistor will be connected SW to GND to discharge the output voltage, this discharge function is turned off when VOUT is fully discharged or the 10ms maximum discharge time elapses.

Application Information

Setting the Output Voltage

The ASP206AS output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.6V. The feedback network is shown below Figure4.

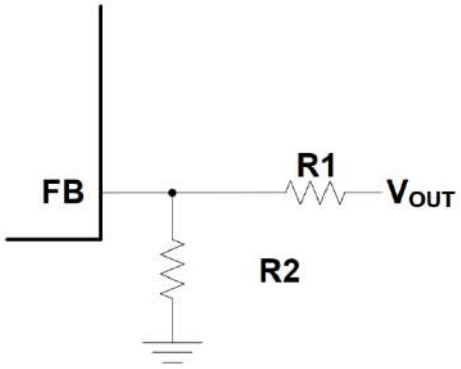


Figure 4: Feedback Network

Choose R_1 and R_2 using Equation:

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \quad (5)$$

Selecting the Inductor

For most applications, use a 1.5μH to 3.3μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a small DC resistance.

For most designs, the inductance value can be derived from Equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{sw}} \quad (6)$$

Where ΔI_L is the inductor ripple current.

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages (4)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)
5	16.2	2.2	3.3	22x2
3.3	10	2.2	3.3	22x2
2.5	6.98	2.2	3.3	22x2
1.8	4.42	2.2	2.2	22x2
1.5	3.3	2.2	2.2	22x2
1.2	2.2	2.2	1.5	22x2
1.05	1.65	2.2	1.5	22x2

Note 4: For a detailed design circuit, please refer to the Typical Application Circuits.

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{sw} \times C_{OUT}}\right) \quad (7)$$

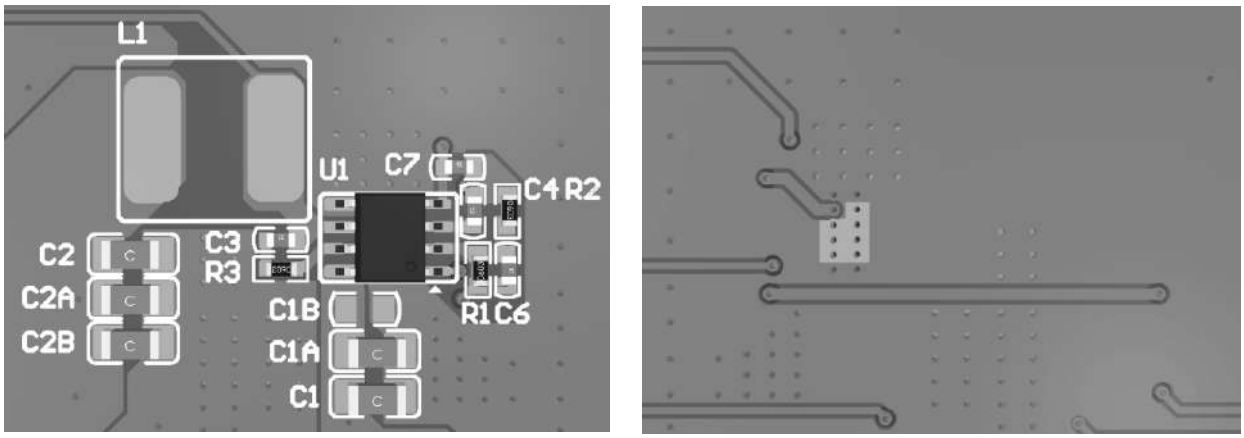
Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The ASP206AS can be optimized for a wide range of capacitance and ESR values.

PCB layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

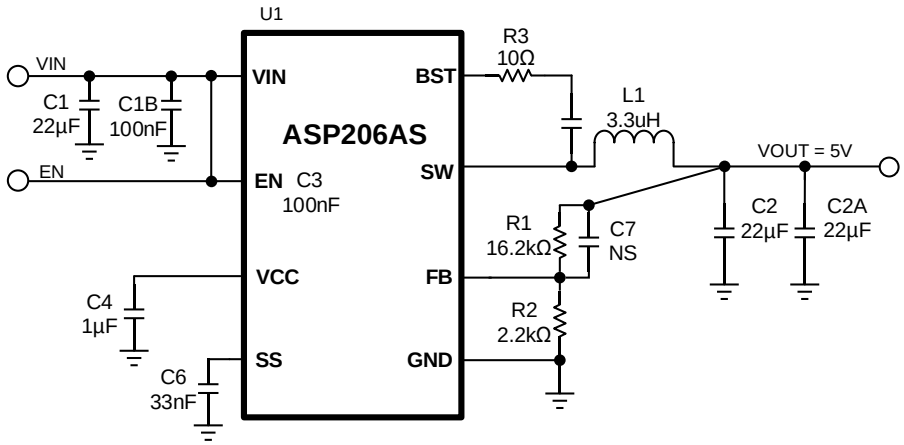
- Place the input capacitor as close to VIN and GND as possible.
- Place the VCC capacitor as close to VCC and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Ensure BST and SW trace as short as possible.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.



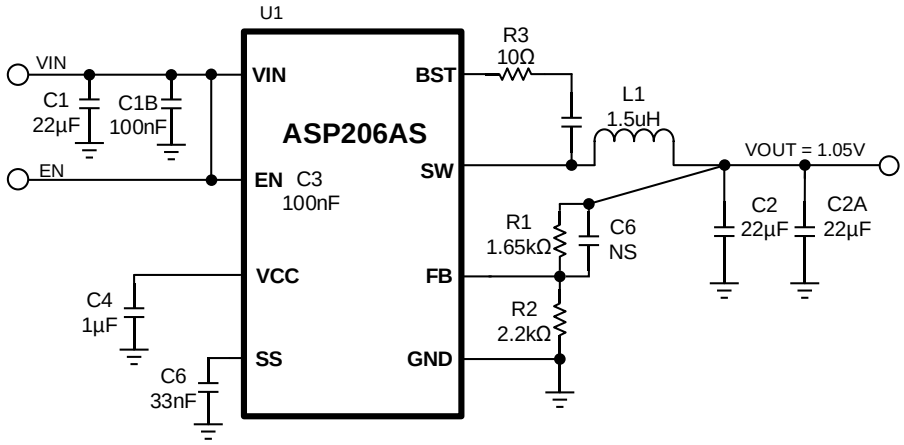
Top Layer **Bottom Layer**

Figure 5 Recommend PCB Layout

Typical Application Circuits



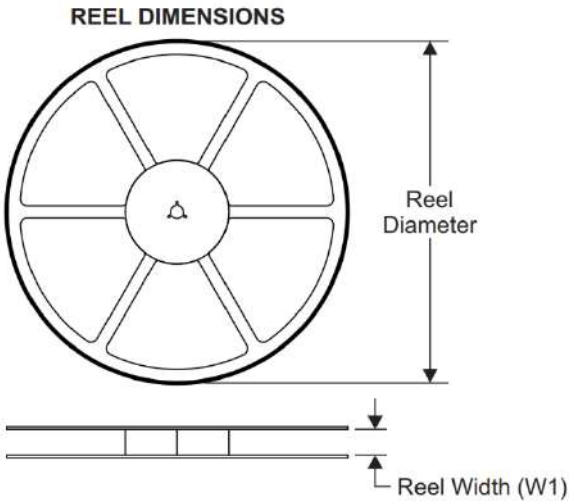
V_{IN}=12V, V_{OUT}=5V/6A

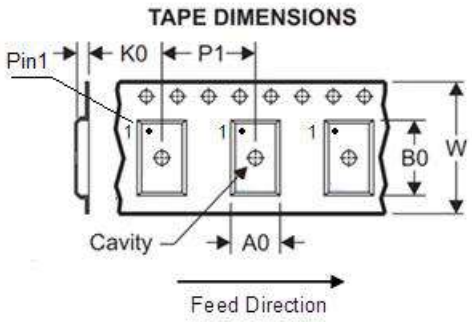


V_{IN}=12V, V_{OUT}=1.05V/6A

Note 5: C7 is optional for better load transient performance.

Tape and Reel Information





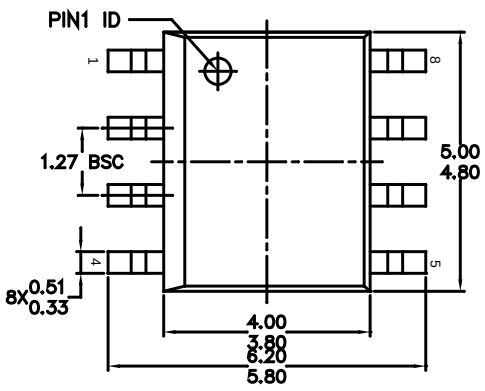
Information (6)

Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
ASP206ASW-R	ESOP-8	8	2500	330	12.4	6.6	5.3	1.9	8	12

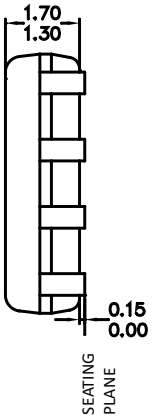
Note 6: Drawing is not to scale.

Detail Package Outline Drawing

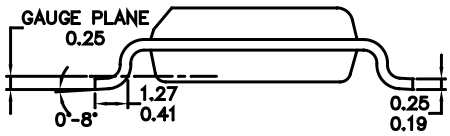
PACKAGE TYPE: ESOP-8



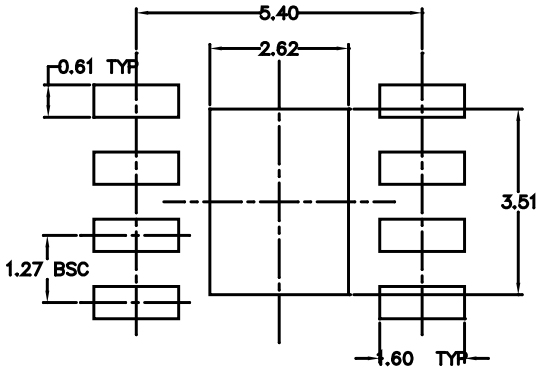
TOP VIEW



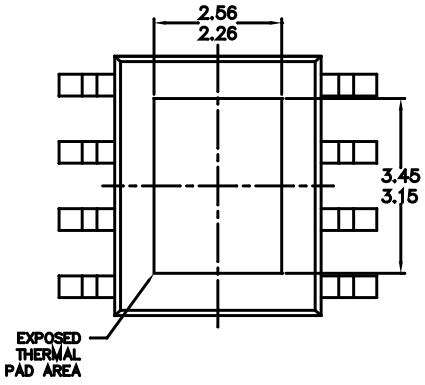
SIDE VIEW



FRONT VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTE:
1) CONTROL DIMENSION IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) EXPOSED TIE BAR FEATURE IS OPTIONAL. EXPOSED PAD SIZE DOES NOT INCLUDE TIE BAR FEATURE.

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