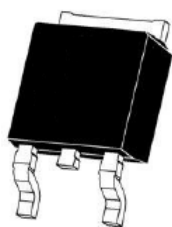


Features

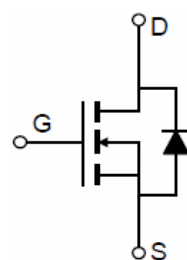
- High ruggedness
- Low $R_{DS(ON)}$
- Low Gate Charge
- Improved dv/dt Capability
- 100% Avalanche Tested

Application

- Synchronous Rectification,
- Li Battery Protect Board, Inverter



TO-252-2L top view



Schematic diagram

Product Summary



V_{DS}	80	V
$R_{DS(on), Typ @ V_{GS}=10V}$	8.4	mΩ
I_D	80	A

Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to source voltage	80	V
I_D	Continuous drain current (@ $T_C=25^{\circ}C$)	80	A
	Continuous drain current (@ $T_C=100^{\circ}C$)	62*	A
I_{DM}	Drain current pulsed (note 1)	320	A
V_{GS}	Gate to source voltage	± 20	V
E_{AS}	Single pulsed avalanche energy (note 2)	240	mJ
E_{AR}	Repetitive avalanche energy (note 1)	20	mJ
dv/dt	Peak diode recovery dv/dt (note 3)	5	V/ns
P_D	Total power dissipation (@ $T_C=25^{\circ}C$)	138.9	W
	Derating factor above 25°C	1.1	W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature	-55 ~ + 150	°C

Thermal characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal resistance, Junction to Ambient	62	°C/W
$R_{\theta JC}$	Thermal resistance, Junction to case	2.2	°C/W

Electrical characteristic ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	80			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	$I_D=250\mu A$, referenced to 25°C		0.06		V/ $^{\circ}\text{C}$
I_{DSS}	Drain to source leakage current	$V_{DS}=80V, V_{GS}=0V$			1	μA
		$V_{DS}=64V, T_J=125^{\circ}\text{C}$			50	μA
I_{GSS}	Gate to source leakage current, forward	$V_{GS}=20V, V_{DS}=0V$			100	nA
	Gate to source leakage current, reverse	$V_{GS}=-20V, V_{DS}=0V$			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	2.9	4	V
$R_{DS(ON)}$	Drain to source on state resistance	$V_{GS}=10V, I_D=40A, T_J=25^{\circ}\text{C}$		8.4	9.9	m Ω
		$V_{GS}=10V, I_D=40A, T_J=125^{\circ}\text{C}$		13.3		m Ω
G_{fs}	Forward transconductance	$V_{DS}=5V, I_D=40A$		55		S
Dynamic characteristics						
C_{iss}	Input capacitance	$V_{GS}=0V, V_{DS}=40V, f=1\text{MHz}$		3988		pF
C_{oss}	Output capacitance			213		
C_{rss}	Reverse transfer capacitance			197		
$t_{d(on)}$	Turn on delay time	$V_{DS}=40V, I_D=30A, R_G=4.7\Omega, V_{GS}=10V$ (note 4,5)		24		ns
t_r	Rising time			67		
$t_{d(off)}$	Turn off delay time			96		
t_f	Fall time			39		
Q_g	Total gate charge	$V_{DS}=64V, V_{GS}=10V, I_D=30A, I_G=3mA$ (note 4,5)		92		nC
Q_{gs}	Gate-source charge			23		
Q_{gd}	Gate-drain charge			34		
R_g	Gate resistance	$V_{DS}=0V$, Scan F mode		5		Ω

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			80	A
I_{SM}	Pulsed source current				320	A
V_{SD}	Diode forward voltage drop.	$I_S=45A, V_{GS}=0V$			1.4	V
t_{rr}	Reverse recovery time	$I_S=30A, V_{GS}=0V, di_F/dt=100A/\mu s$		39		ns
Q_{rr}	Reverse recovery charge			60		nC

※. Notes

1. Repeattive rating : pulse width limited by junction temperature.
2. $L=0.5mH, I_{AS}=31A, V_{DD}=40V, R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
3. $I_{SD} \leq 30A, di/dt = 100A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J=25^{\circ}\text{C}$
4. Pulse Test : Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

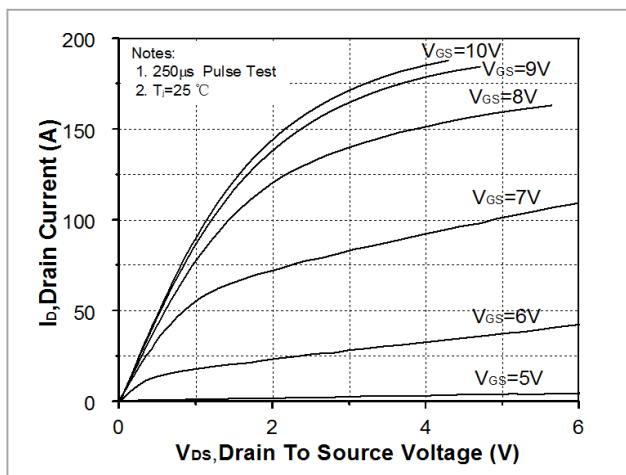


Fig. 2. Transfer Characteristics

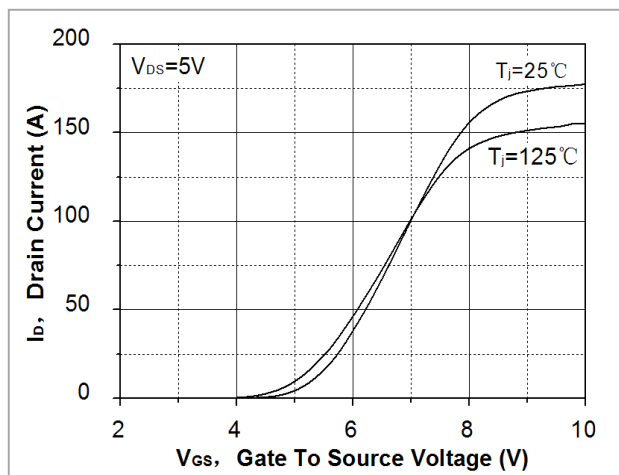


Fig. 3. On-resistance variation vs. drain current and gate voltage

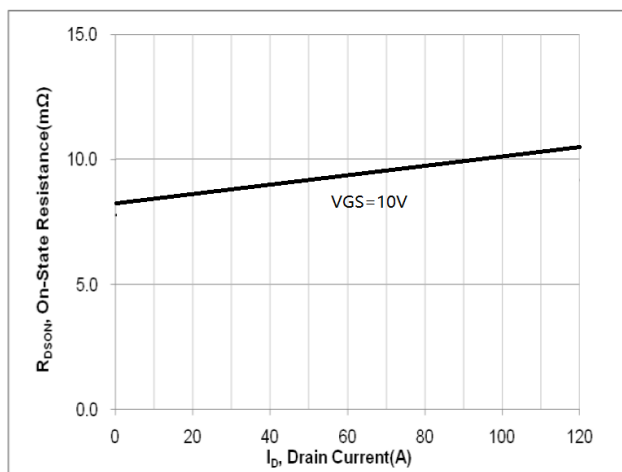


Fig. 4. On-state current vs. diode forward voltage

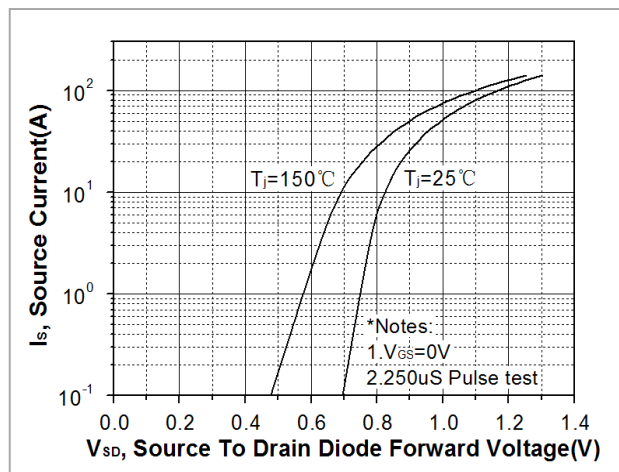


Fig 5. Breakdown voltage variation vs. junction temperature

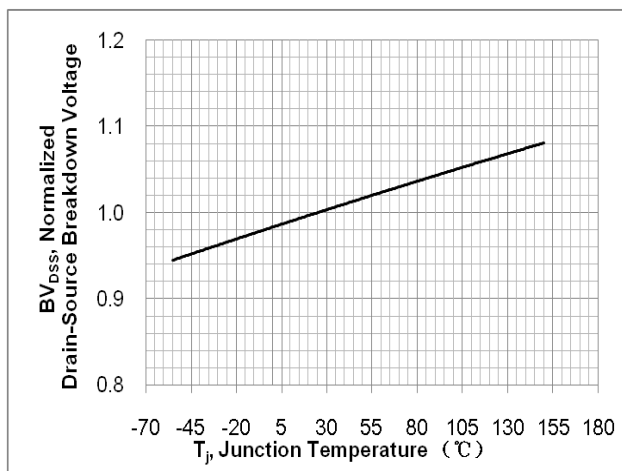


Fig. 6. On-resistance variation vs. junction temperature

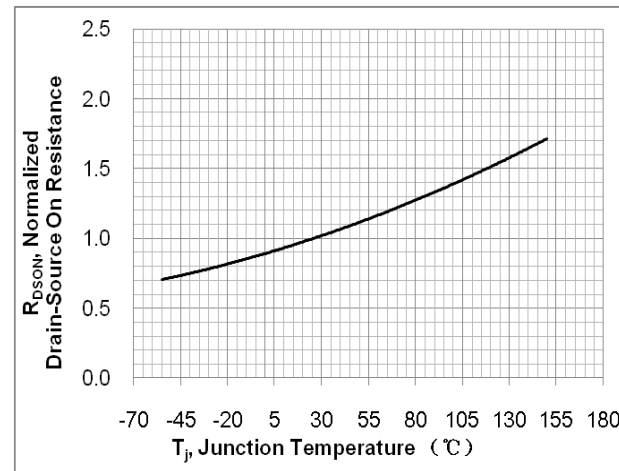


Fig. 7. Gate charge characteristics

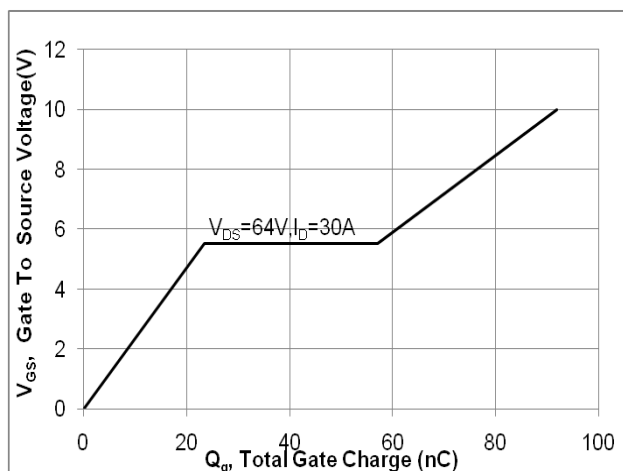


Fig. 8. Capacitance Characteristics

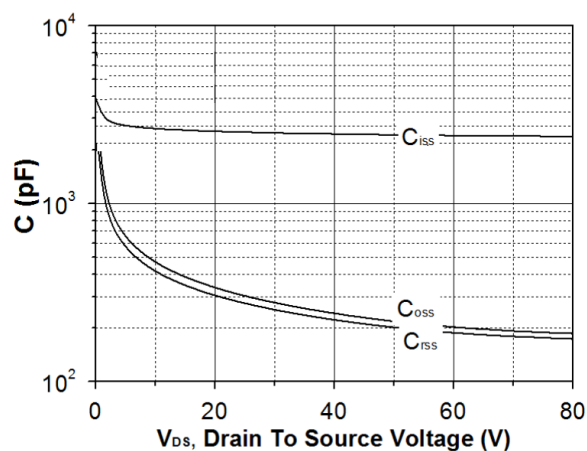


Fig. 9. Maximum safe operating area

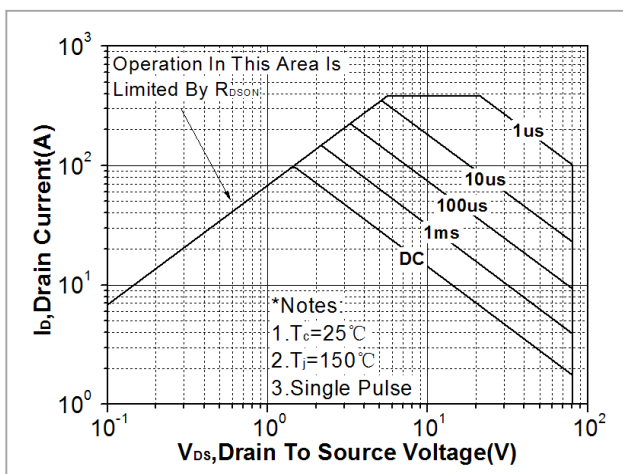


Fig. 10. Maximum drain current vs. case temperature

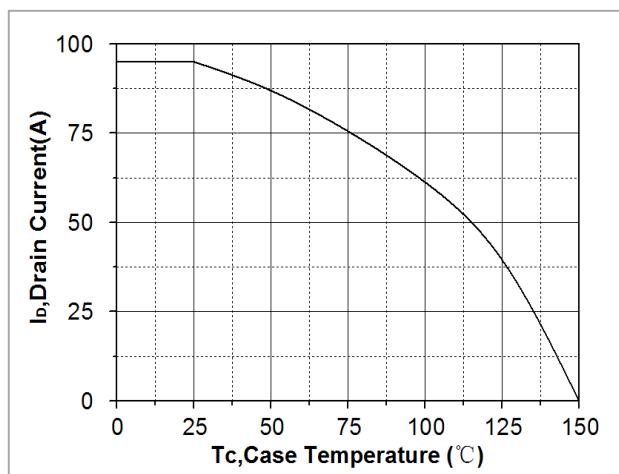


Fig. 11. Transient thermal response curve

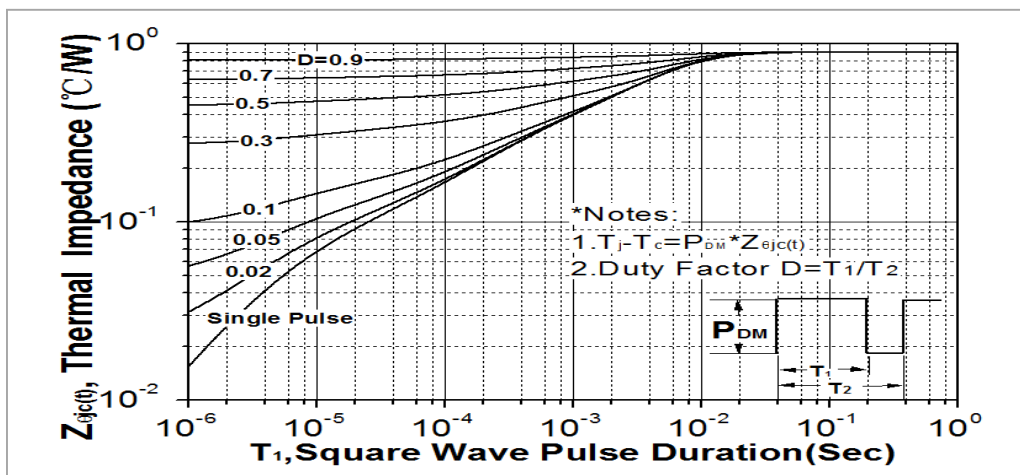


Fig. 12. Gate charge test circuit & waveform

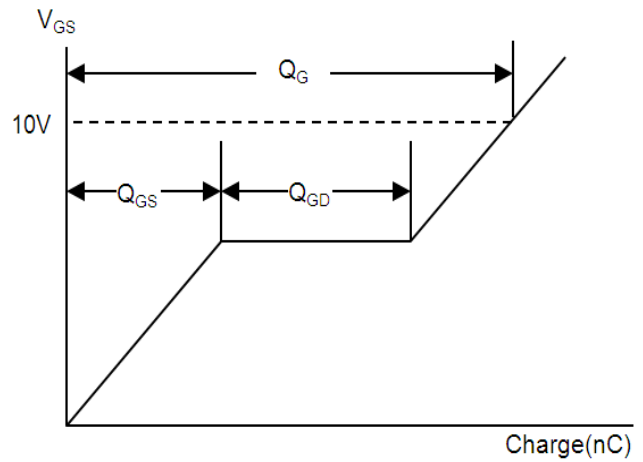
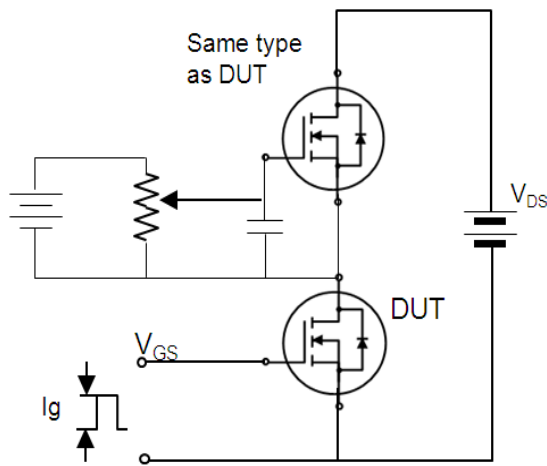


Fig. 13. Switching time test circuit & waveform

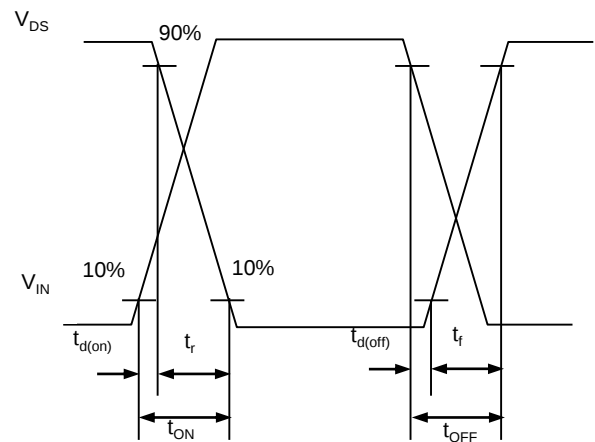
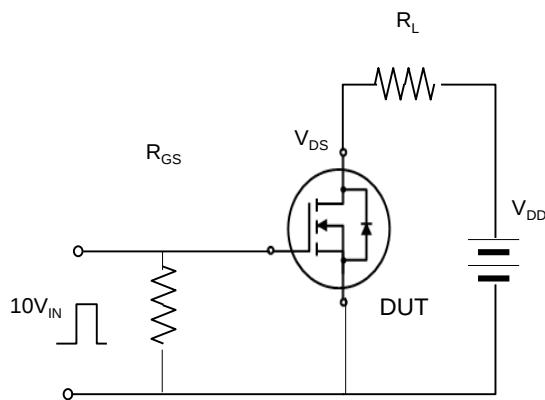


Fig. 14. Unclamped Inductive switching test circuit & waveform

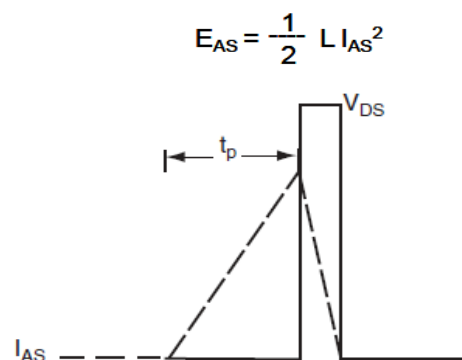
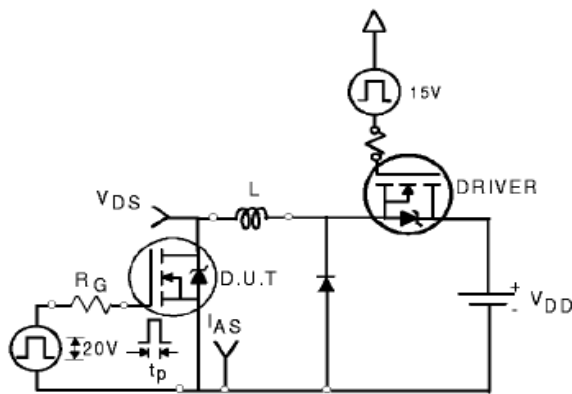
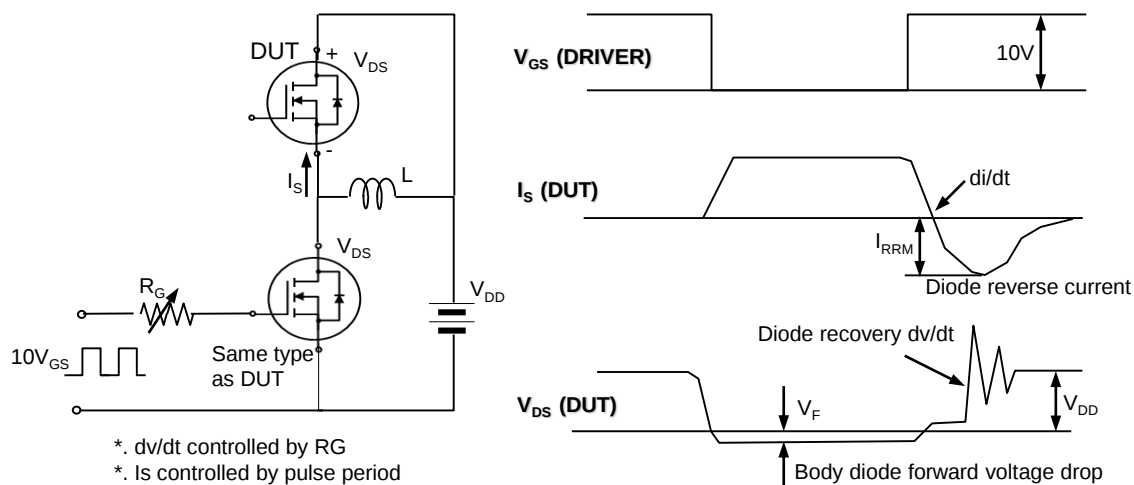
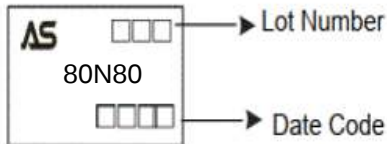


Fig. 15. Peak diode recovery dv/dt test circuit & waveform

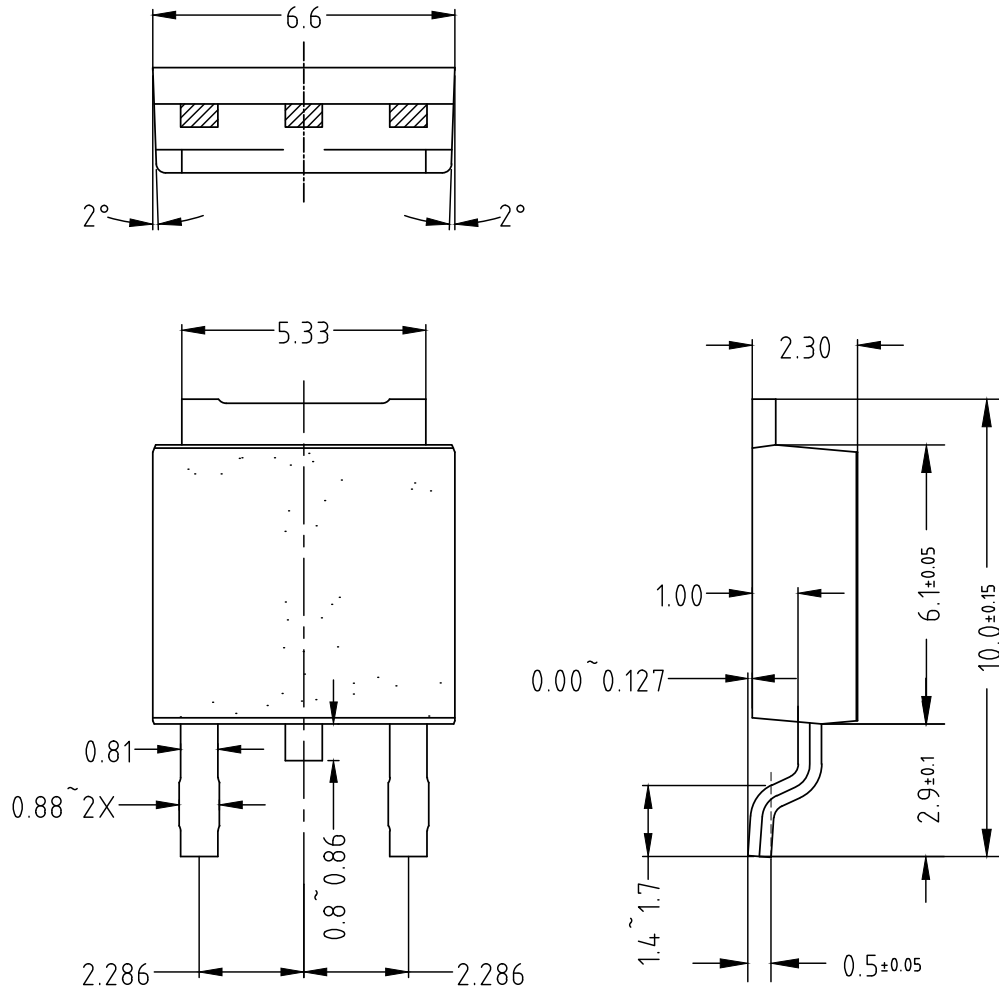


Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM80N80KQ-R	80N80	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	 The marking diagram shows a rectangular package with the following markings: 'AS' logo, '80N80', a four-digit 'Lot Number', and a four-digit 'Date Code'.

TO-252



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