

Feature

- High density cell design for lower $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

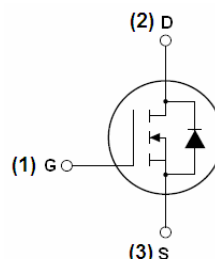
Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply



Product Summary

V_{DS}	100	V
$R_{DS(on), Typ @ V_{GS}=10V}$	32	mΩ
I_D	33	A



Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	33	A
Drain Current-Pulsed (Note 1)	I_{DM}	132	A
Maximum Power Dissipation($T_c=25^{\circ}\text{C}$)	P_D	70	W
Single pulse avalanche energy (Note 2)	E_{AS}	96	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.4	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient (PCB mount)	$R_{\theta JA}$	62	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1	1.6	2.4	V
Drain-Source On-State Resistance ^(Note 3)	R _{DS(ON)}	V _{GS} =10V, I _D =12A	-	32	35	mΩ
		V _{GS} =4.5V, I _D =12A	-	33	45	
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =15A	-	11	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =25V,V _{GS} =0V, f=1.0MHz	-	2160	-	pF
Output Capacitance	C _{oss}		-	202	-	pF
Reverse Transfer Capacitance	C _{rss}		-	183	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, ID=20A, V _{GS} =10V,R _{GEN} =10Ω	-	29	-	nS
Turn-on Rise Time	t _r		-	13	-	nS
Turn-Off Delay Time	t _{d(off)}		-	58.2	-	nS
Turn-Off Fall Time	t _f		-	13.4	-	nS
Total Gate Charge	Q _g	V _{DS} =80V,I _D =20A V _{GS} =10V	-	55	-	nC
Gate-Source Charge	Q _{gs}		-	15	-	nC
Gate-Drain Charge	Q _{gd}		-	20	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Reverse Recovery Time	T _{rr}	Tj=25℃ , IF=10A, di/dt=100A/uS ^(note3)	-	58	-	nS
Reverse Recovery Charge	Q _{rr}		-	110	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. E_{AS} condition : $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_{GS}=10V, L=0.5mH, R_g=25\Omega$
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production.



Characteristics Curves

Figure 1 Output Characteristics

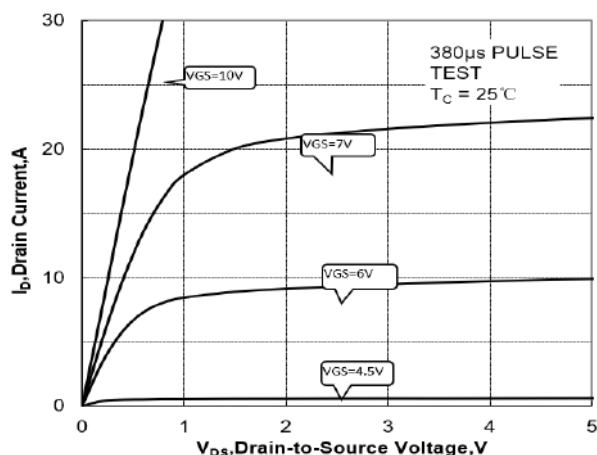


Figure 2 Transfer Characteristics

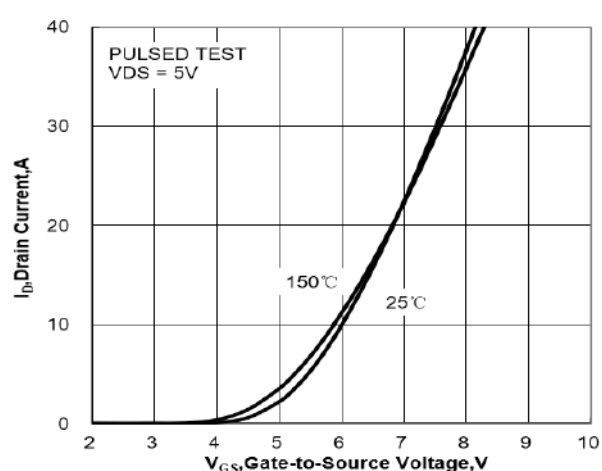
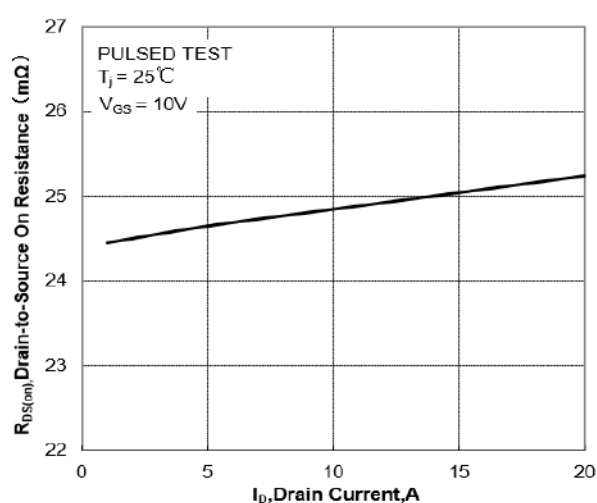
Figure 3 On-Resistance vs. I_D and V_{GS} 

Figure 4 On-Resistance vs. Junction Temperature

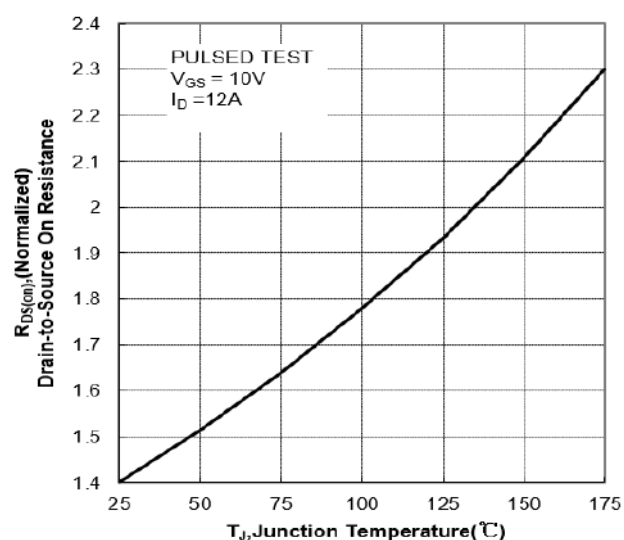
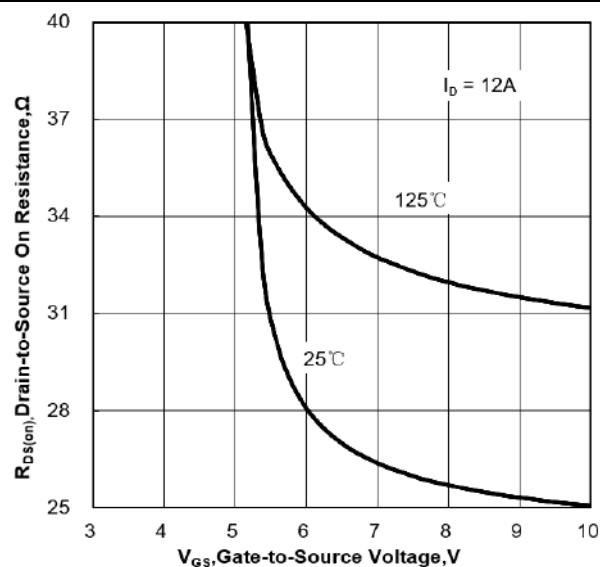
Figure 5 On-Resistance vs. V_{GS} 

Figure 6 Body Diode Forward Voltage

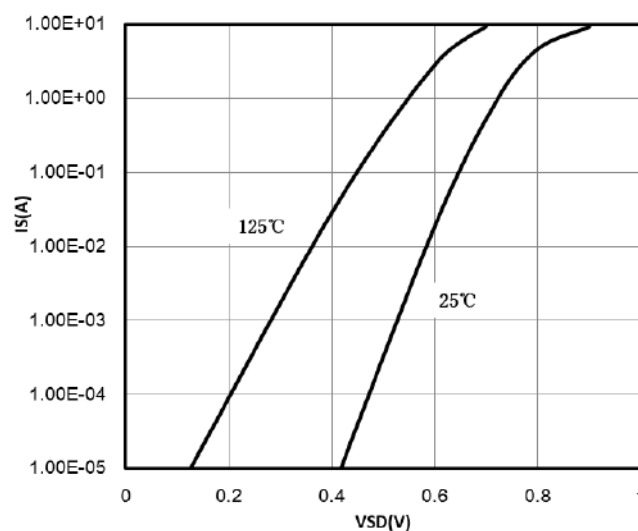


Figure 7 Gate-Charge Characteristics

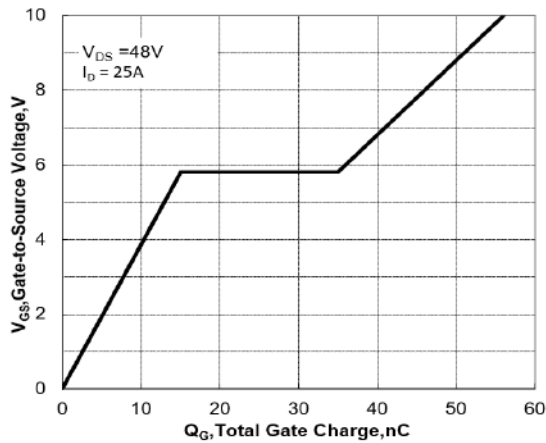


Figure 8 Capacitance Characteristics

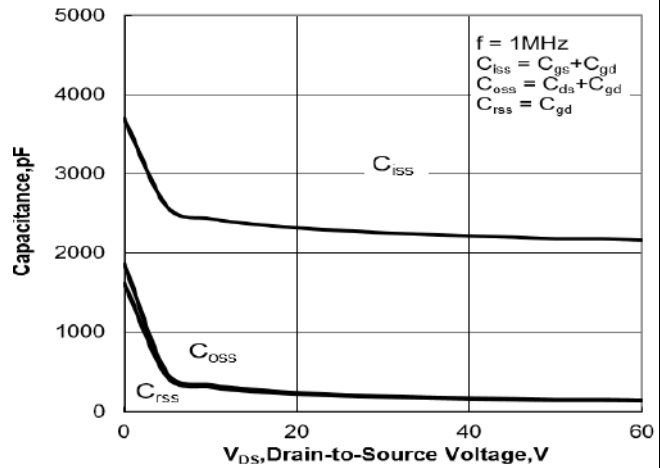


Figure 9 Maximum Forward Biased Safe Operation Area

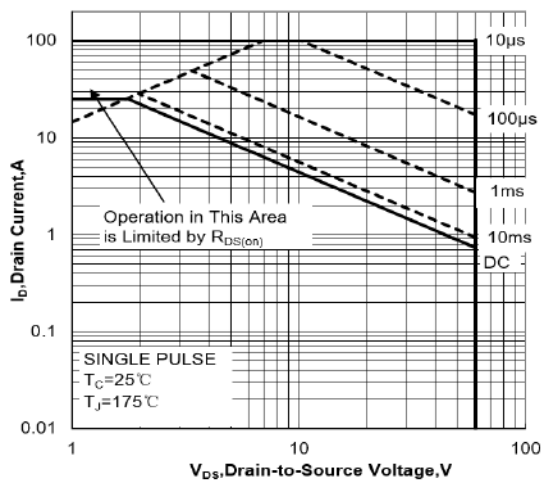


Figure 10 Single Pulse Power Rating Junction-to-Ambient

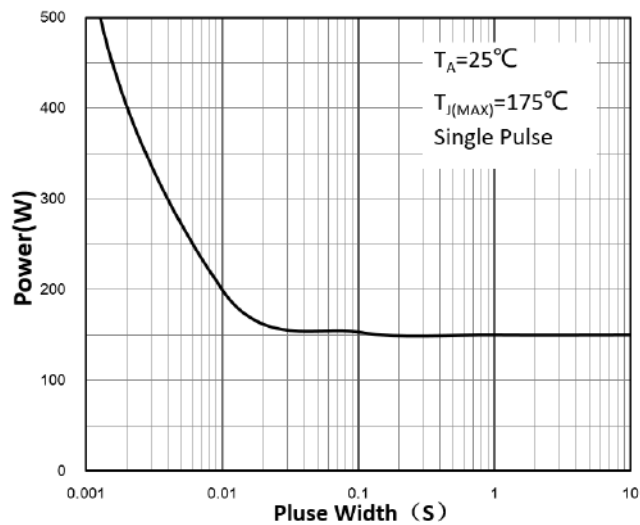
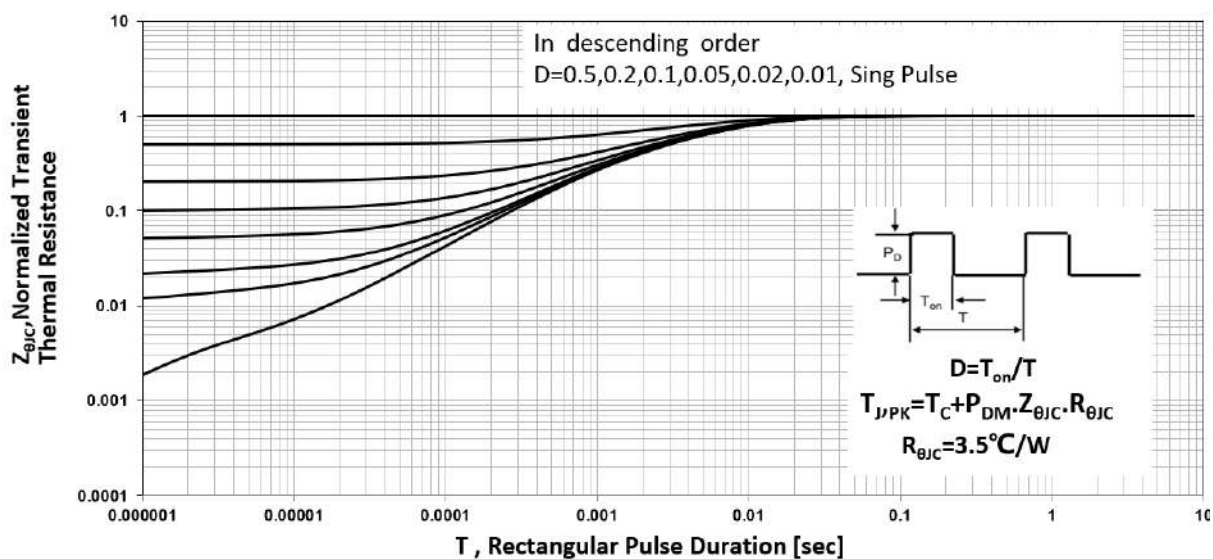
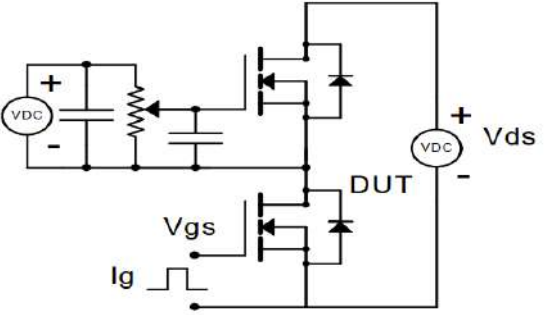
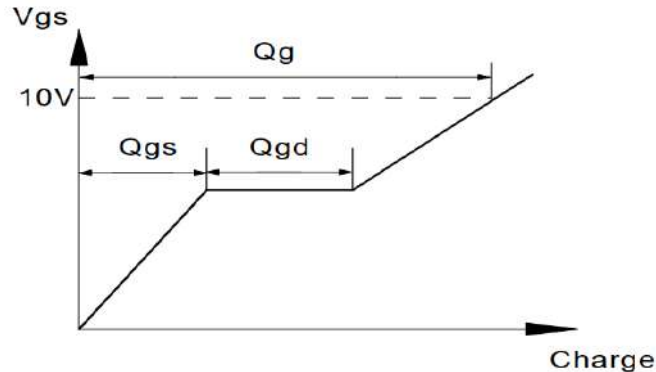
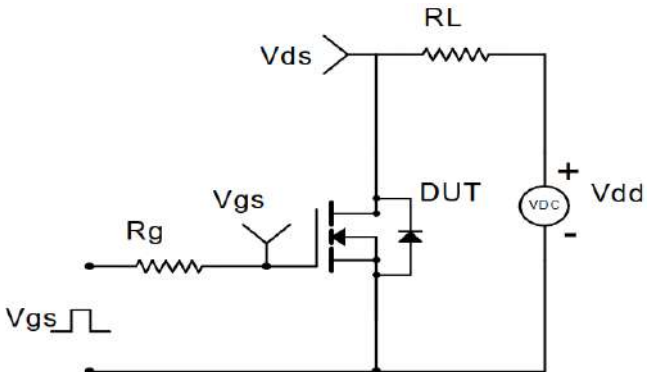
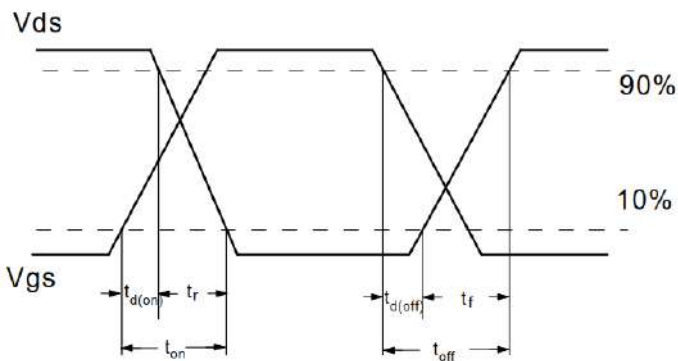
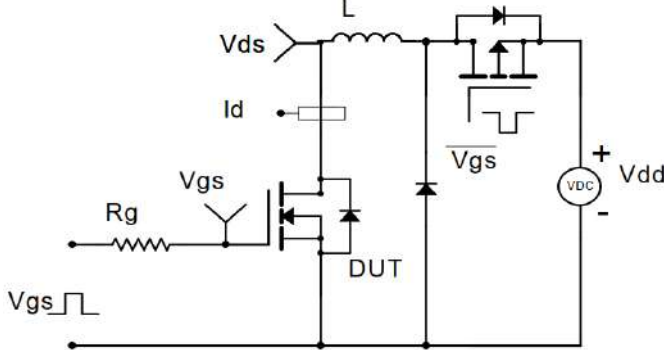
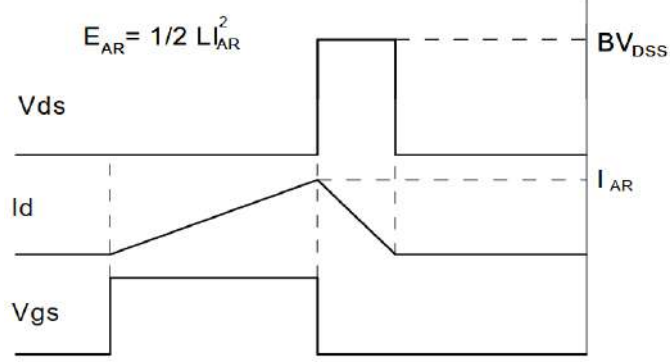
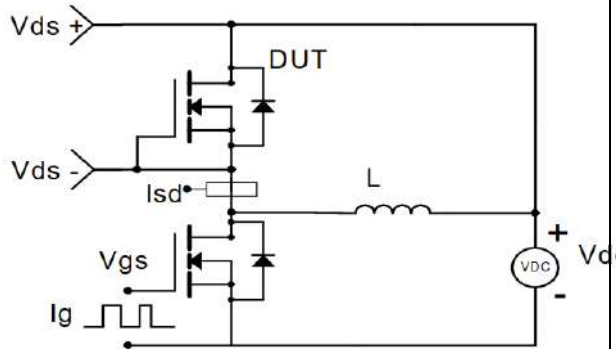
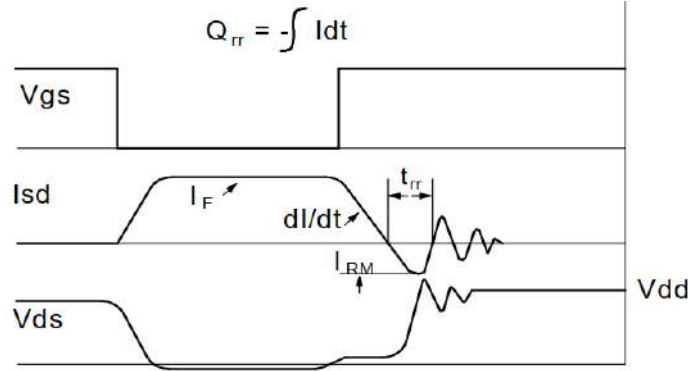


Figure 11 Normalized Maximum Transient Thermal Impedance



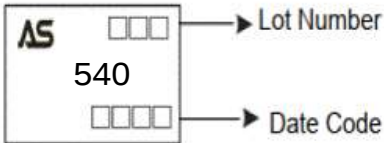


Test Circuit and Waveform

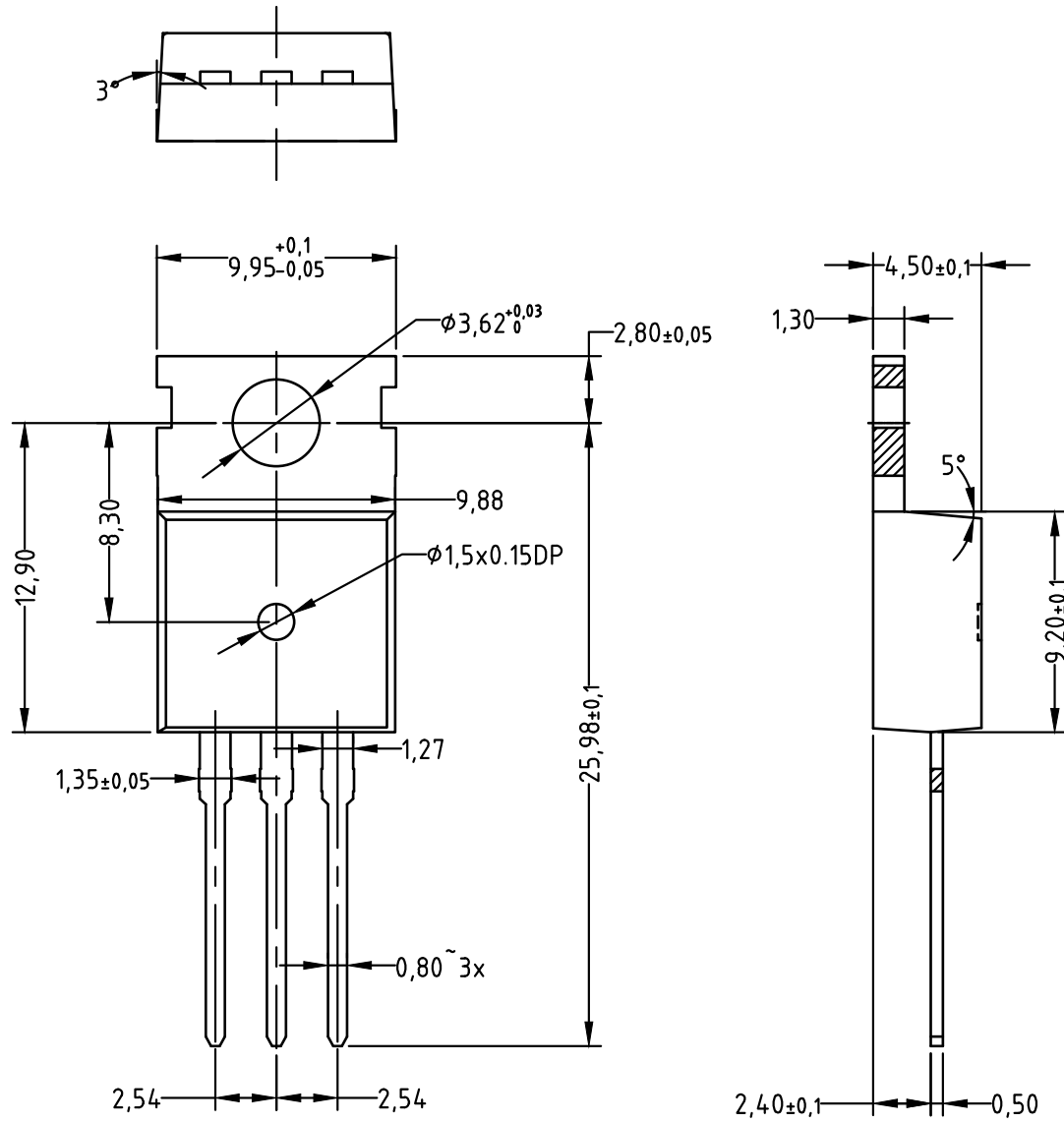
Gate Charge Test Circuit 	Gate Charge Test Waveform 
Resistive Switching Test Circuit 	Resistive Switching Test Waveforms 
Unclamped Inductive Switching (UIS) Test Circuit 	Unclamped Inductive Switching (UIS) Test Waveforms 
Diode Recovery Test Circuit 	Diode Recovery Test Waveforms 

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM540P-T	540	TO-220	Tube	50/Tube

PACKAGE	MARKING
TO-220	 The diagram shows a TO-220 package with the following markings: 'AS' in the top left, '540' in the center, and two sets of four squares (representing Lot Number and Date Code) in the top right and bottom right respectively. Arrows point from the text 'Lot Number' and 'Date Code' to their respective square groups.

TO-220



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