

Features

- Magnachip's MV MOSFET technology
- N-channel, Normal level
- 100% UIS and Rg tested
- Maximum 175°C junction temperature
- AEC-Q101 qualified

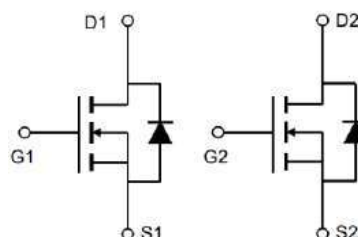
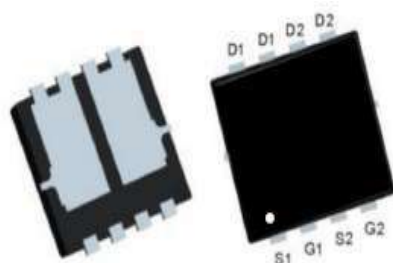
Application

- Motor inveter
- Switching applications

Product Summary



V_{DS}	40	V
$R_{DS(on),Max}@ V_{GS}=10\text{ V}$	7	mΩ
I_D	60	A



PDFN 5x6 - 8

ABSOLUTE MAXIMUM RATINGS, at $T_C = 25^\circ\text{C}$, unless otherwise specified

PARAMETER		SYMBOL	RATING	UNIT
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain current	$T_C=25^\circ\text{C}$ (Silicon Limited)	I_D	60	A
	$T_C=25^\circ\text{C}$ (Package Limited)		35	A
	$T_C=100^\circ\text{C}$		43	A
Pulsed drain current	$T_C=25^\circ\text{C}$	I_{DM}	240	A
Total power dissipation	$T_C=25^\circ\text{C}$	P_{tot}	54	W
	$T_C=100^\circ\text{C}$		27	W
Avalanche energy, single pulse		E_{AS}	50	mJ
Operating and storage temperature		T_j, T_{stg}	- 55 ~ 175	$^\circ\text{C}$

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATING	UNIT
Thermal resistance, junction - case	$R_{\theta JC}$	2.8	$^\circ\text{C/W}$
Thermal resistance, junction - ambient	$R_{\theta JA}$	100	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS (T_j = 25°C)
STATIC CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Drain-source breakdown voltage	V _{(BR)DSS}	40	-	-	V	V _{GS} =0 V, I _D =250 μA
Gate threshold voltage	V _{GS(th)}	2.45	-	3.95	V	V _{DS} =V _{GS} , I _D =250 μA
Zero gate voltage drain current	I _{DSS}	-	-	1	μA	V _{DS} =40 V, V _{GS} =0 V
Gate-source leakage current	I _{GSS}	-	-	± 100	nA	V _{GS} =±20 V, V _{DS} =0 V
Drain-source on-state resistance	R _{DS(on)}	-	-	7	mΩ	V _{GS} =10 V, I _D =17.5 A
Gate resistance	R _G	-	2.3	-	Ω	f=1MHz
Transconductance	g _{fs}	-	54	-	S	V _{DS} =20 V, I _D =17.5 A

DYNAMIC CHARACTERISTICS

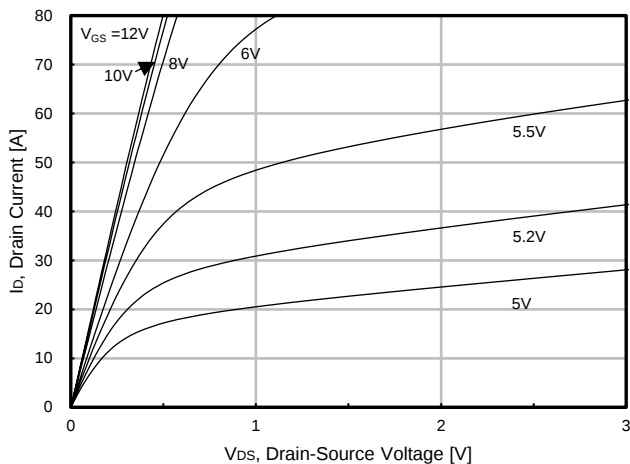
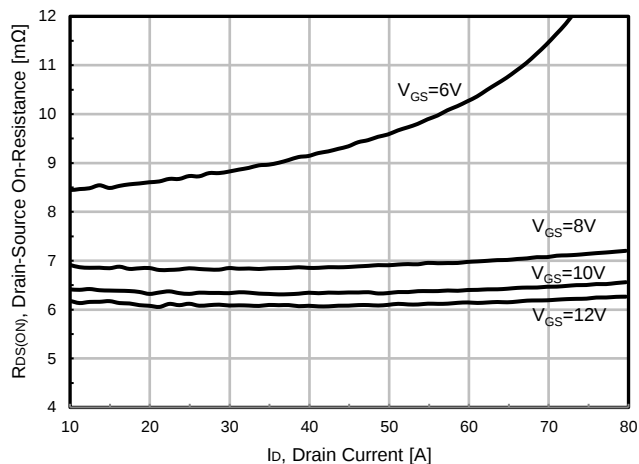
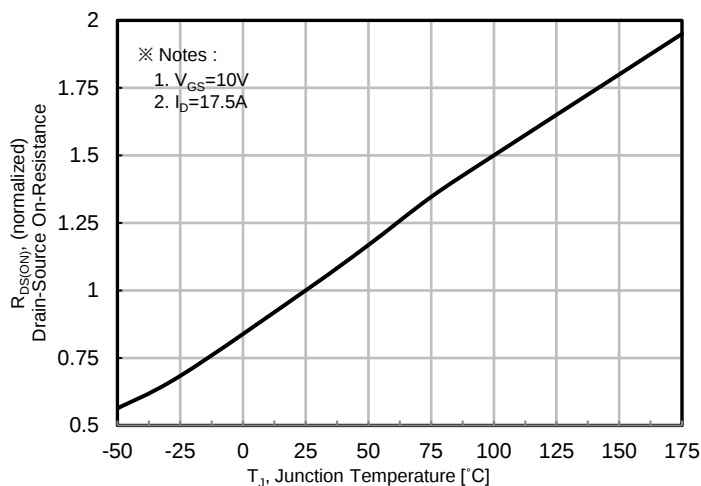
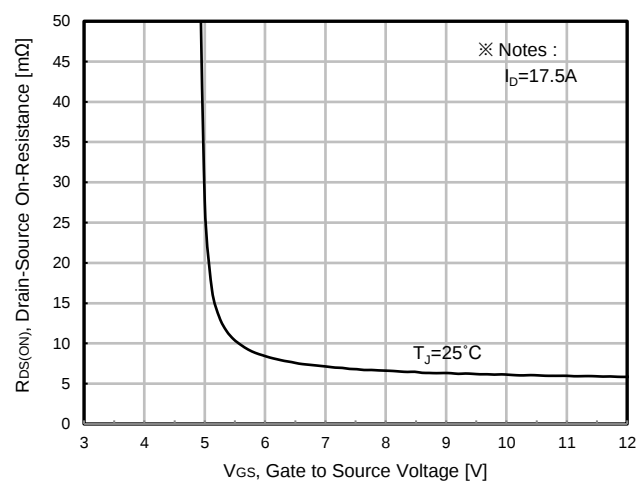
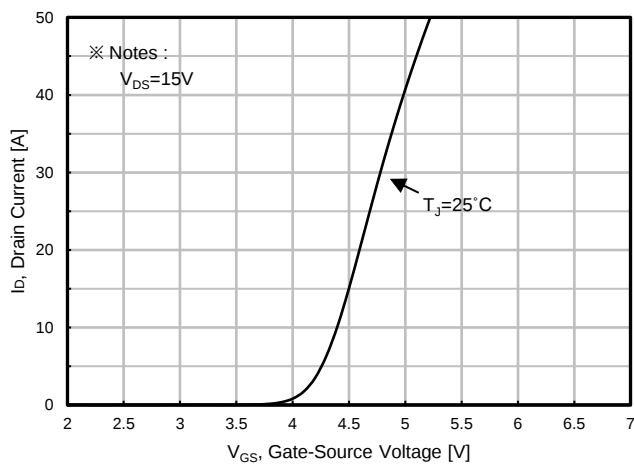
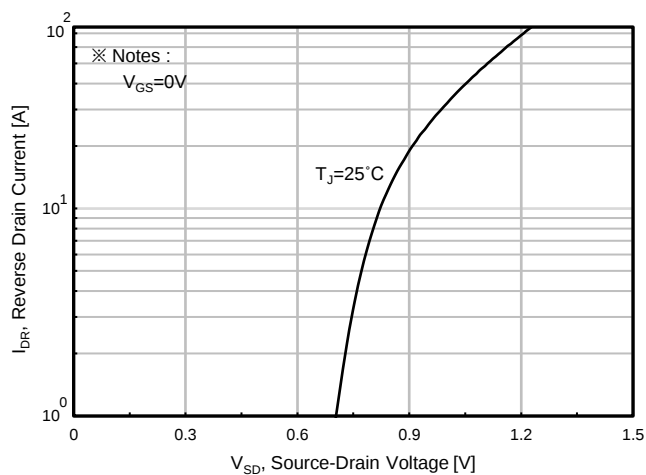
PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Input capacitance	C _{iss}	-	1658	-	pF	V _{GS} =0 V, V _{DS} =20 V, f=1 MHz
Output capacitance	C _{oss}	-	445	-	pF	V _{GS} =0 V, V _{DS} =20 V, f=1 MHz
Reverse transfer capacitance	C _{rss}	-	41	-	pF	V _{GS} =0 V, V _{DS} =20 V, f=1 MHz
Turn-on delay time	t _{d(on)}	-	16.5	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =17.5 A, R _{G,ext} =3Ω
Rise time	t _r	-	11	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =17.5 A, R _{G,ext} =3Ω
Turn-off delay time	t _{d(off)}	-	27	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =17.5 A, R _{G,ext} =3Ω
Fall time	t _f	-	8.8	-	ns	V _{DD} =20 V, V _{GS} =10 V, I _D =17.5 A, R _{G,ext} =3Ω

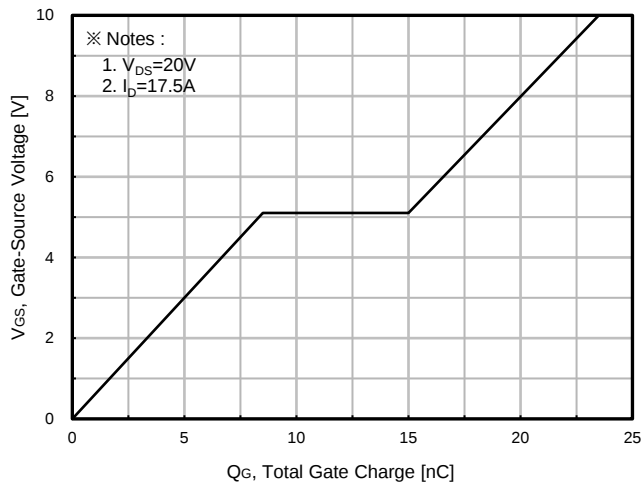
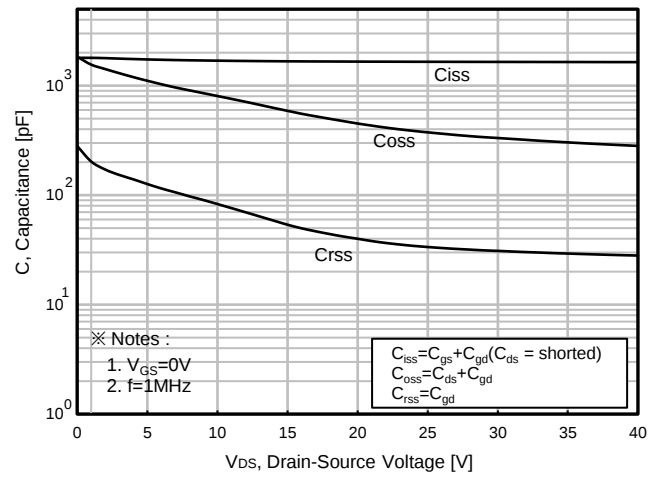
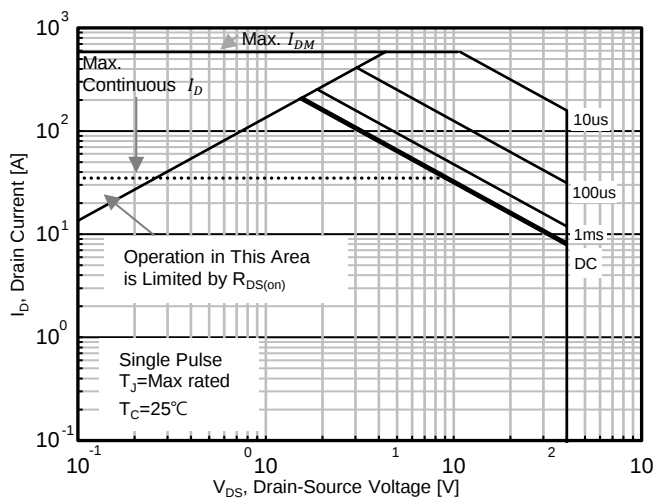
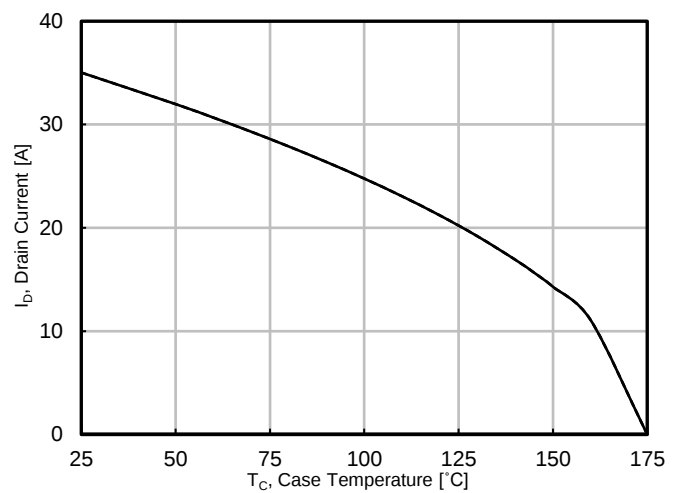
GATE CHARGE CHARACTERISTICS

PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Gate to source charge	Q _{gs}	-	8.5	-	nC	V _{DD} =20 V, I _D =17.5 A, V _{GS} =0 to 10 V
Gate charge at threshold	Q _{gs(th)}	-	4.9	-	nC	V _{DD} =20 V, I _D =17.5 A, V _{GS} =0 to 10 V
Gate to drain charge	Q _{gd}	-	3.1	-	nC	V _{DD} =20 V, I _D =17.5 A, V _{GS} =0 to 10 V
Switching charge	Q _{sw}	-	6.6	-	nC	V _{DD} =20 V, I _D =17.5 A, V _{GS} =0 to 10 V
Gate charge total	Q _g	-	23.5	-	nC	V _{DD} =20 V, I _D =17.5 A, V _{GS} =0 to 10 V
Gate plateau voltage	V _{plateau}	-	5.1	-	V	V _{DD} =20 V, I _D =17.5 A, V _{GS} =0 to 10 V

SOURCE-DRAIN DIODE

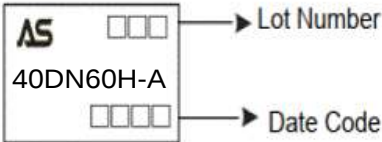
PARAMETER	Symbol	Min.	Typ.	Max.	Unit	Conditions / Note
Diode continuous forward current	I _S	-	-	35	A	-
Diode pulse current	I _{S,pulse}	-	-	244	A	pulsed; t _p ≤ 10 μs
Diode forward voltage	V _{SD}	-	0.9	1.2	V	V _{GS} =0 V, I _F =17.5 A
Reverse recovery time	t _{rr}	-	57.1	-	ns	I _F =17.5 A, dI _F /dt=100 A/μs
Reverse recovery charge	Q _{rr}	-	51.7	-	nC	I _F =17.5 A, dI _F /dt=100 A/μs

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

Fig. 1. Output Characteristics (25°C)

Fig. 2. Static On-Resistance Variation

Fig. 3. On-Resistance vs. Junction Temperature

Fig. 4. On-Resistance vs. Gate to source Voltage

Fig. 5. Transfer Characteristics

Fig. 6. Body Diode Forward Voltage Variation with Source Current and Temperature

ELECTRICAL CHARACTERISTICS DIAGRAMS (25 °C, unless otherwise noted)

Fig. 7. Gate Charge

Fig. 8. Capacitance

Fig. 9. Safe Operating Area, Junction-to-Ambient

Fig. 10. Maximum Drain vs. Case Temperature

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM40DN60HQ-R	40DN60H-A	PDFN5*6-8	Tape&Reel	4000/Reel

PACKAGE	MARKING
PDFN5*6-8	 AS □□□ → Lot Number 40DN60H-A □□□□ → Date Code

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