

650V N-Channel Super-Junction MOSFET



Features

- Much lower On-resistance $R_{DS(ON)}$
- Low C_{rss}
- Fast switching
- Improved dv/dt capability
- Electrostatic Discharge (ESD)

Applications

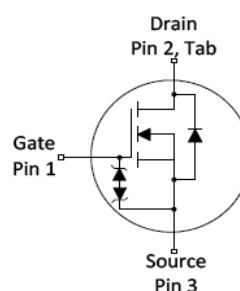
- LED/LCD/PDP TV and monitor Lighting
- Solar/Renewable/UPS-Micro Inverter System
- Charger
- Power Supply

Product Summary

VDS	650	V
$R_{DS(on)}$, Typ. @ $V_{GS}=10V$	341	m Ω
ID	11	A



TO-220F



Schematic Diagram

Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	650	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	11	A
	- Continuous ($T_C = 100^\circ\text{C}$)	7.9	A
I_{DM}	Drain Current - Pulsed (Note 1)	44	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy	300	mJ
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	118	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.15	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

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Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μ A	650	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	--	--	1	μ A
		V _{DS} = 520V, T _C = 125°C	--	--	10	μ A
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30V, V _{DS} = 0 V	--	--	1	μ A
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-1	μ A

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μ A	2.0	3.0	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3.4A	--	341	360	m Ω

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	780	-	pF
C _{oss}	Output Capacitance		--	597	-	pF
C _{rss}	Reverse Transfer Capacitance		--	17.4	-	pF
R _G	Gate resistance	F = 1.0 MHz, Open drain	--	3.8	-	Ω

Switching Characteristics

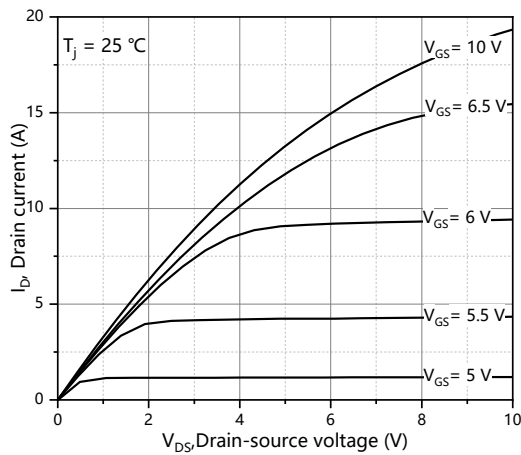
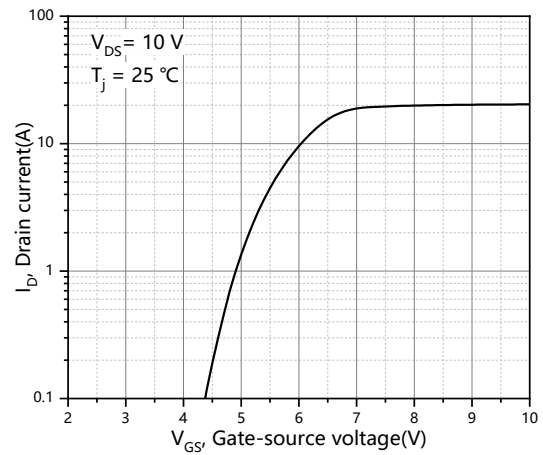
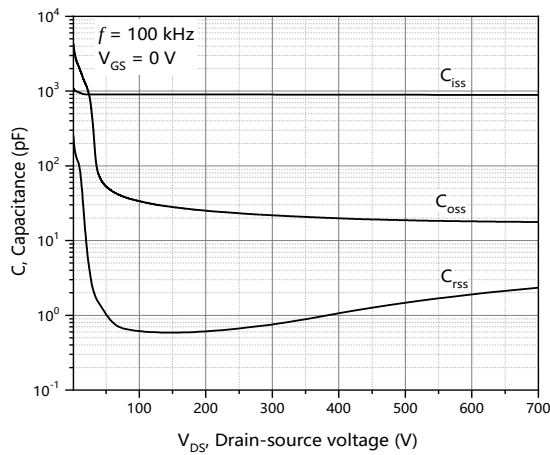
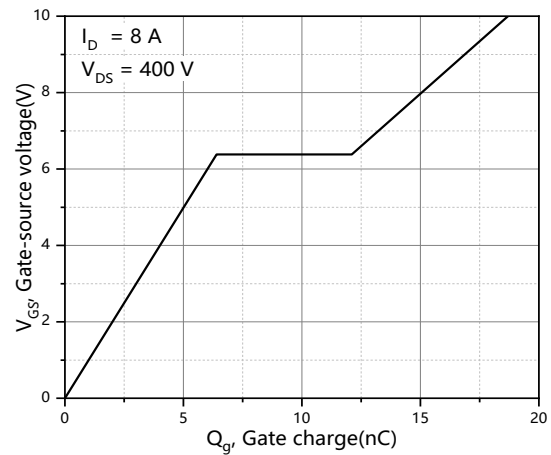
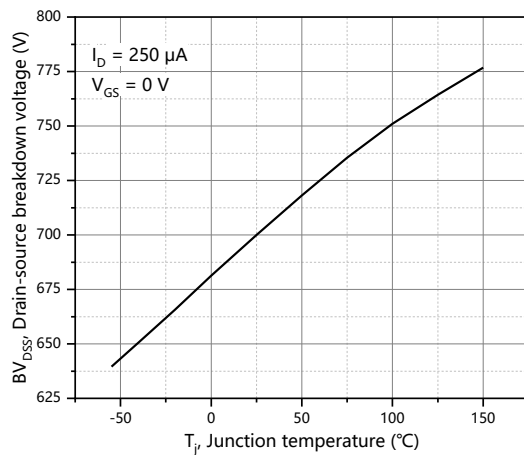
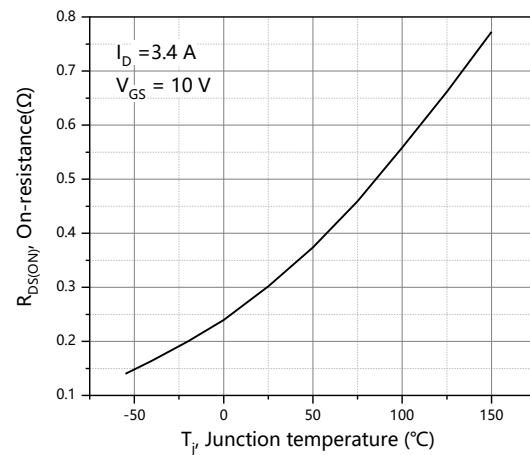
t _{d(on)}	Turn-On Delay Time	V _{GS} = 10 V, V _{DS} = 400 V, R _G = 25 Ω , I _D = 4A	--	16	--	ns
t _r	Turn-On Rise Time		--	35	--	ns
t _{d(off)}	Turn-Off Delay Time		--	75	--	ns
t _f	Turn-Off Fall Time		--	38	--	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 4A, V _{GS} = 10V	--	18.9	--	nC
Q _{gs}	Gate-Source Charge		--	2.54	--	nC
Q _{gd}	Gate-Drain Charge		--	6.09	--	nC

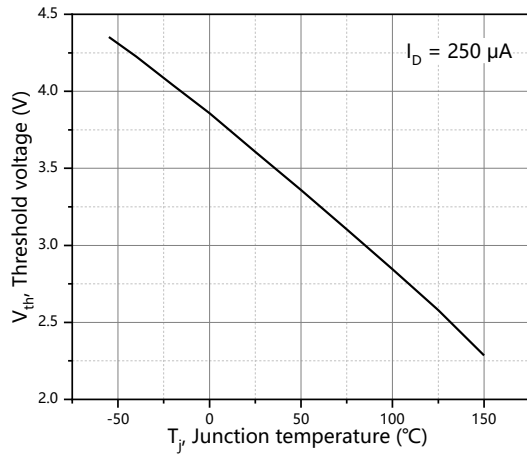
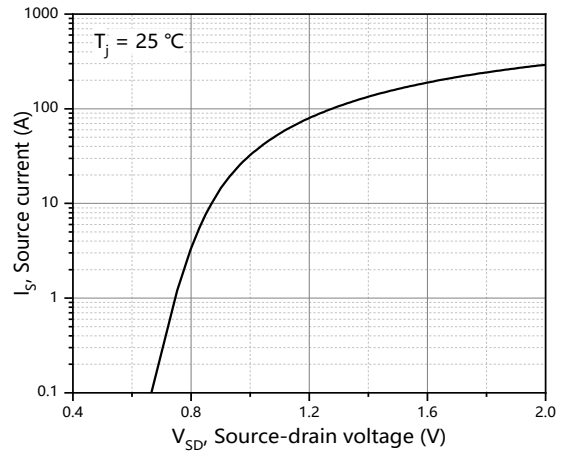
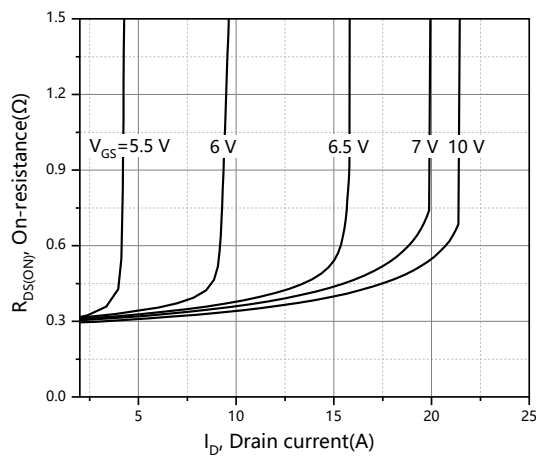
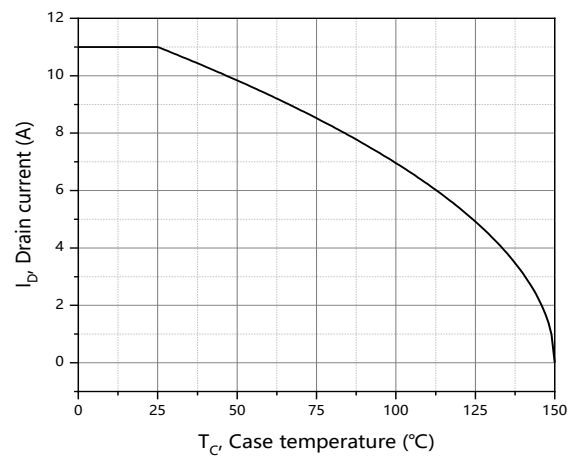
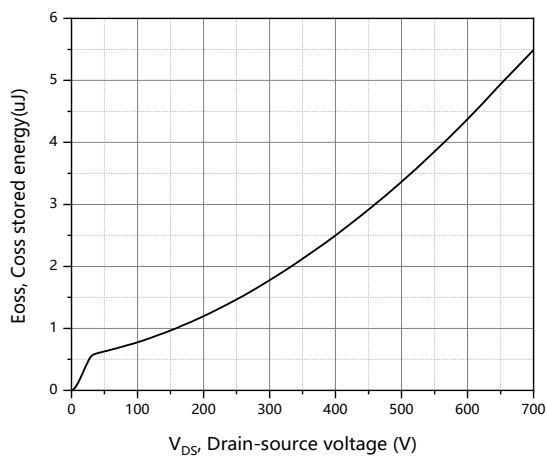
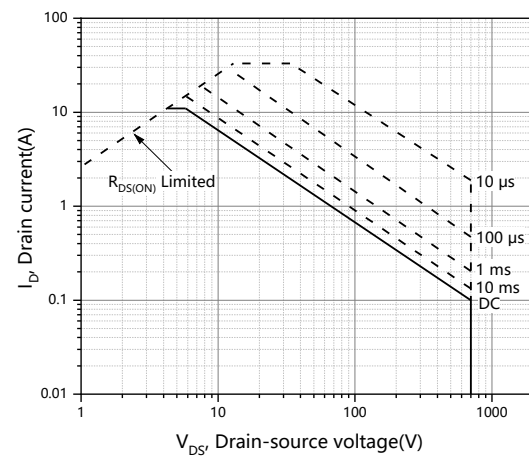
Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	11	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	44	A
V _{SD}	Drain to Source Diode Forward Voltage, V _{GS} = 0V, I _{SD} = 3A, T _J = 25°C	0.32	0.8	1.2	V
t _{rr}	Body Diode Reverse Recovery Time, I _F = 3.4A, dI/dt = 100A/ μ s	--	208	--	nS
Q _{rr}	Body Diode Reverse Recovery Charge, I _F = 3.4A, dI/dt = 100A/ μ s	--	2.9	--	nC

Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. EAS condition: T_J = 25°C, V_{DD} = 50V, V_G = 10V, R_G = 25 Ω , L = 0.5mH,
3. Pulse Test: Pulse Width $\leq$ 300 μ s, Duty Cycles $\leq$ 0.5%

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Electrical Characteristics Diagrams

Figure 1. Typ. output characteristics

Figure 2. Typ. transfer characteristics

Figure 3. Typ. capacitances

Figure 4. Typ. gate charge

Figure 5. Drain-source breakdown voltage

Figure 6. Drain-source on-state resistance

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Figure 7. Threshold voltage

Figure 8. Forward characteristic of body diode

Figure 9. Drain-source on-state resistance

Figure 10. Drain current

Figure 11. Typ. Coss stored energy

Figure 12. Safe operation area Tc=25 °C

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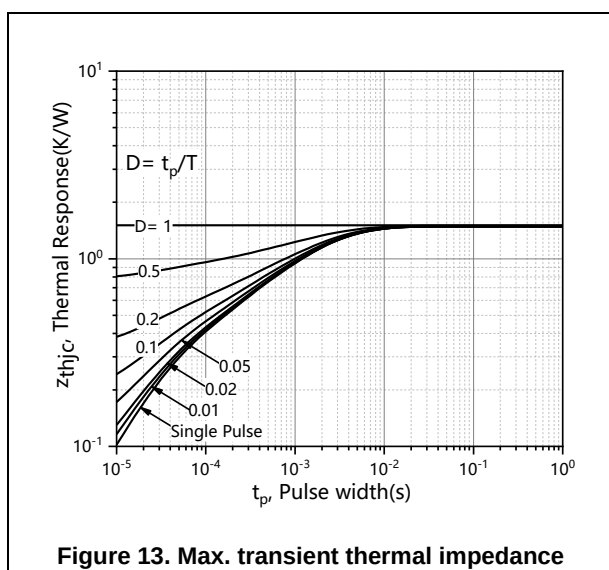


Figure 13. Max. transient thermal impedance

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Test circuits and waveforms

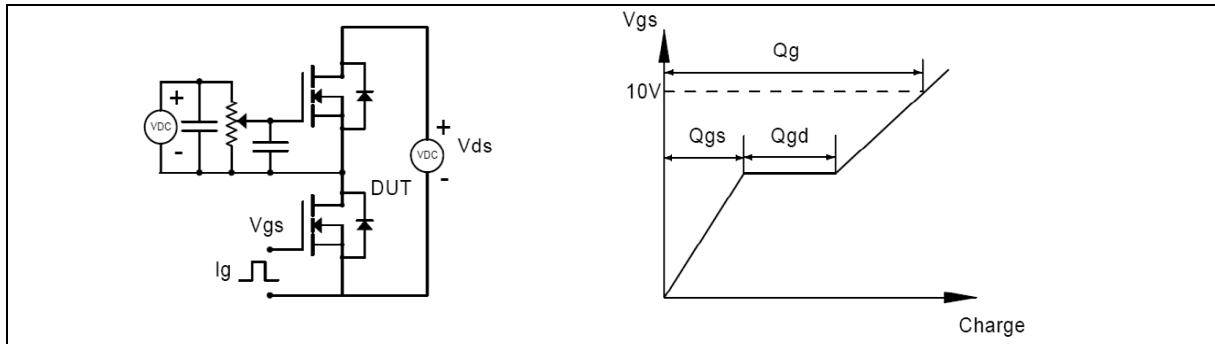


Figure 1. Gate charge test circuit & waveform

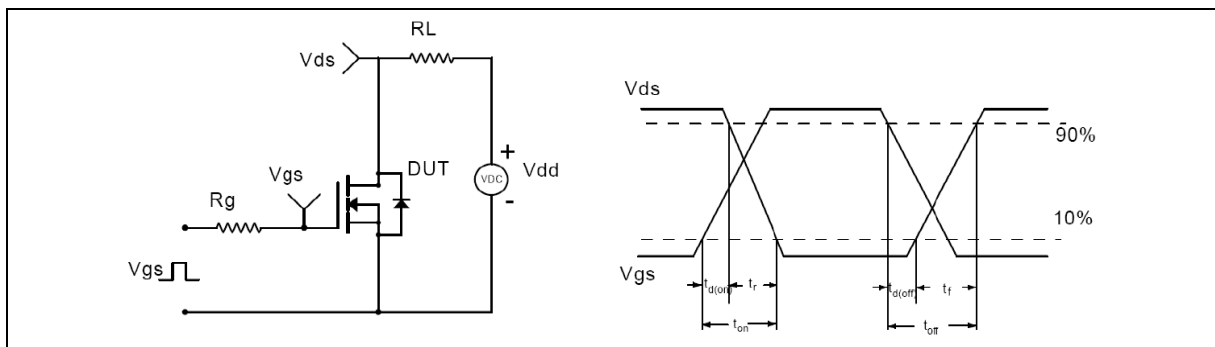


Figure 2. Switching time test circuit & waveforms

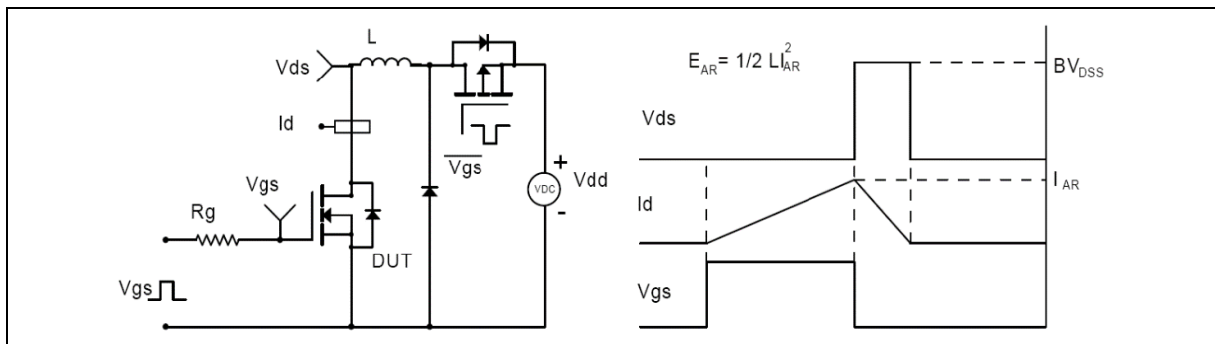


Figure 3. Unclamped inductive switching (UIS) test circuit & waveforms

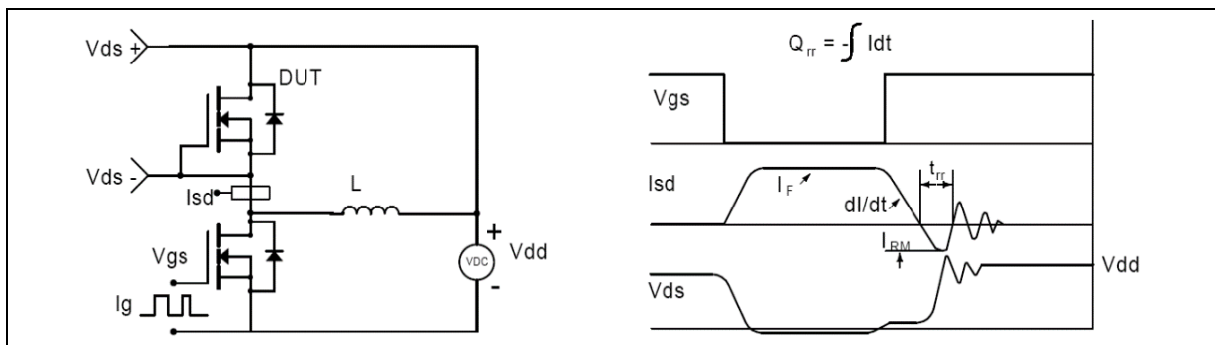
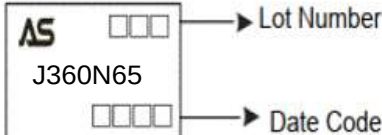


Figure 4. Diode reverse recovery test circuit & waveforms

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Ordering and Marking Information

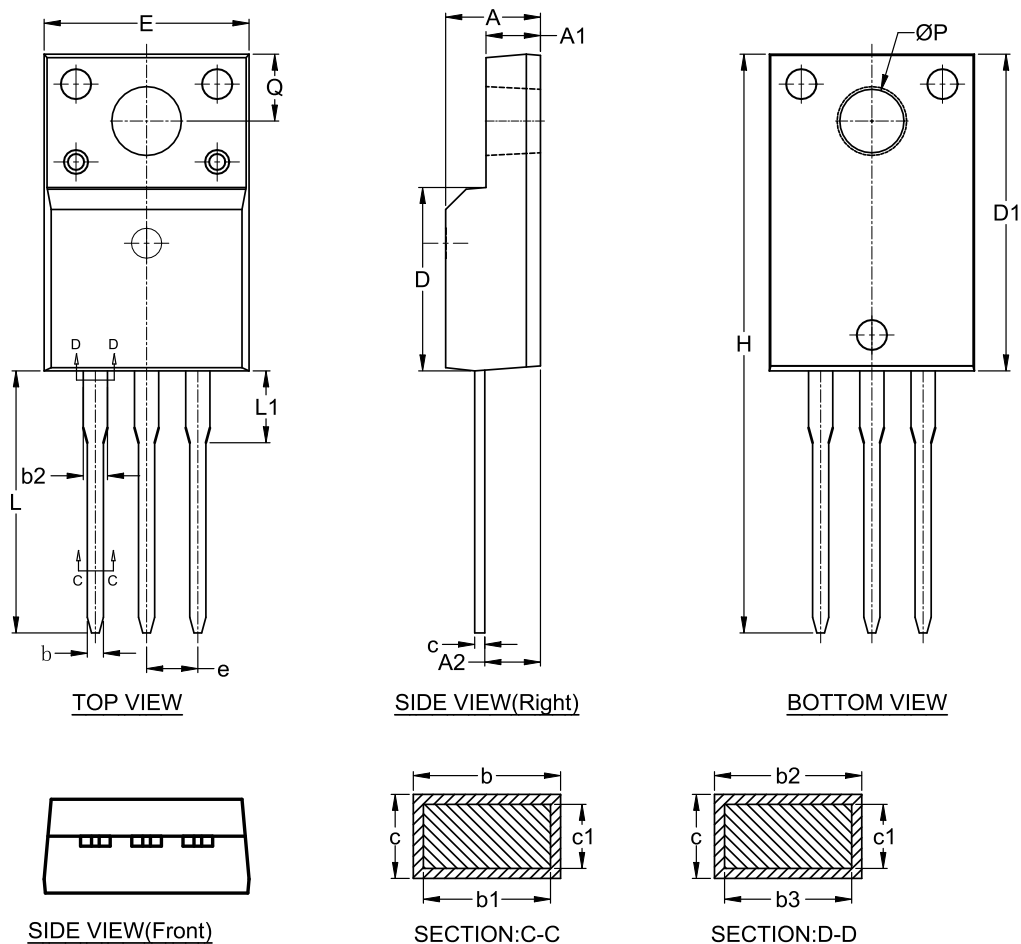
Ordering Device No.	Marking	Package	Packing	Quantity
ASJ360N65F1HE-T	J360N65	TO-220F	Tape&Reel	50/Reel

PACKAGE	MARKING
TO-220F	 The diagram shows a rectangular marking area on a TO-220F package. It contains the ASDsemi logo (AS) in the top left, followed by two empty boxes for the Lot Number. Below these is the part number J360N65, followed by four empty boxes for the Date Code. Arrows point from the text 'Lot Number' and 'Date Code' to their respective boxes.

Package Description

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TO-220F



DIM SYMBOL	MIN.	NOM.	MAX.
A	4.600	4.700	4.800
A1	2.600	2.700	2.800
A2	2.660	2.760	2.860
b	0.740	0.840	0.940
b1	0.700	0.800	0.900
b2	1.140	1.240	1.340
b3	1.100	1.200	1.300
c	0.440	0.540	0.640
c1	0.400	0.500	0.600
D	9.090	9.190	9.290
D1	15.770	15.870	15.970
E	10.060	10.160	10.260
e	2.540 BSC.		
H	28.800	29.000	29.200
L	12.930	13.130	13.330
L1	3.400	3.600	3.800
ØP	3.080	3.180	3.280
Q	3.150	3.350	3.550

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