Features

- High Efficiency: Up to 96%
- 2.5V to 5.5V Input Voltage Range
- 1MHz Constant Frequency Operation
- Up to 5.0A Current Output
- No Schottky Diode Required
- Over temperature Protected
- Low Quiescent Current: 40μA
- Short Circuit Protection
- Inrush Current Limit and Soft Start
- DFN3*3-10 package

Applications

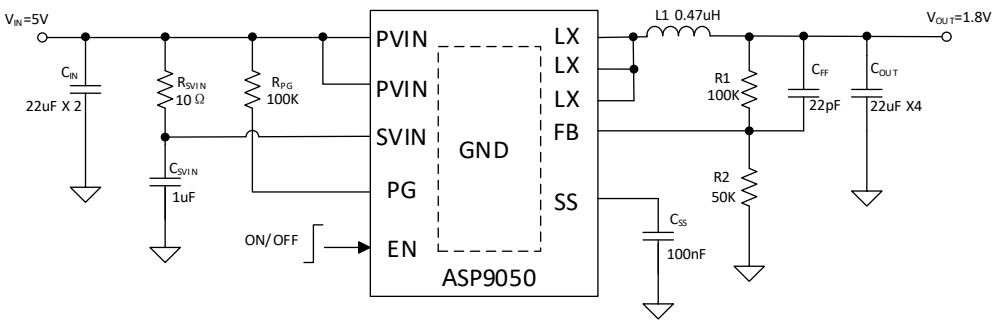
- Cellular and Smart Phones
- Wireless and DSL Modems
- PDAs
- Portable Instruments
- SSD
- PC Cards

General Description

The ASP9050 is a high-efficiency ECOT Mode synchronous buck regulator using a constant frequency. The device is available in an adjustable version. Supply current with no load is 40uA and drops to <1uA in shutdown. The 2.5V to 5.5V input voltage range makes the ASP9050 ideally suited for single Li-Ion battery powered applications. High duty cycle provides low dropout operation, extending battery life in portable systems. PWM/ PFM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally set at 1MHz, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.6V feedback reference voltage.

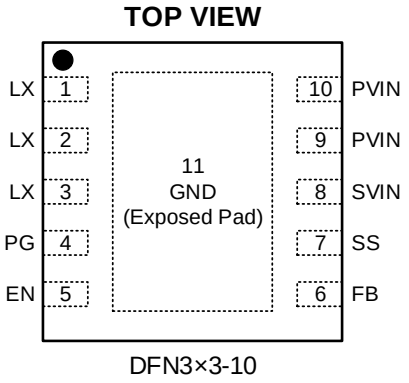
The ASP9050 is offered in a low profile 10-pin, thin DFN3*3-10 package, and is available in an adjustable version.

Typical Application Circuit



Basic Application Circuit

Pin Description



Top Marking: AREAA (device code: AR, E=year code, AA= lot number code)

Pin Description

Pin	Name	Function
1/2/3	LX	Power Switch Output. It is the switch node connection to Inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches.
4	PG	Power good indicator pin. Open drain output if the output is within 90% of regulation; low otherwise.
5	EN	Chip Enable Pin. Drive EN above 1.5V to turn on the part. Drive EN below 0.3V to turn it off. Do not leave EN floating.
6	FB	Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.
7	SS	Soft-Start programming pin. Connect a capacitor from this pin to ground to program the soft-Start time. T_{SS}=Max 600us, C_{SS}*0.6V/10uA).
8/9/10	VIN	Power Supply Input. Must be closely decoupled to GND with a 22µF or greater ceramic capacitor.
11	GND/EPAD	Ground Pin

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V_{IN} voltage	-0.3	6.5	V
EN voltage	-0.3	6.5	V
LX voltage	-0.3	V_{IN}+0.3V	V
FB voltage	–0.3	6	V
PG voltage	–0.3	6	V
SS voltage	-0.3	3	V
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	–55	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	2.5	5.5	V
Output current	0	5	A

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	40.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	°C/W
$R_{\theta JC}$	Junction-to-case (Bottom) thermal resistance	2.8	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1)(2)

(V_{IN}=V_{EN}=3.6V, T_A = 25°C, unless otherwise noted.)

Parameter	Test Conditions	Min	Typ.	Max	Unit
Input Voltage Range		2.5		5.5	V
Supply Current (Quiescent)	V_{EN} =3.0V		40	80	uA
Supply Current (Shutdown)	V_{EN} =0 or EN = GND		0.1	1	uA
Feedback Voltage		0.585	0.600	0.615	V
High-Side Switch On-Resistance	I_{SW}=100mA		50		mΩ
Low-Side Switch On-Resistance	I_{SW}=-100mA		40		mΩ
Valley Switch Current Limit			8		A
Over Voltage Protection Threshold			6		V
Switching Frequency			1		MHz
Maximum Duty Cycle	VFB=90% V_{REF}		88		%
Minimum Off-Time			65		nS
SS Charge Current			10		uA
EN Rising Threshold		1.4			V
EN Falling Threshold				0.8	V
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage		2.4	2.5	V
	Shutdown V_{IN} Voltage	2.2	2.3		V
	Hysteresis V_{IN} voltage		200		mV
PG vs. VFB Threshold	VFB Falling (Fault)		91		%V_{REF}
	VFB Rising (Good)		95		%V_{REF}
	VFB Rising (Fault)		108		% V_{REF}
	VFB Falling (Good)		104		%V_{REF}
	Hysteresis VFB voltage		28		mV
Thermal Shutdown			150		°C
Thermal Hysteresis			20		°C

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

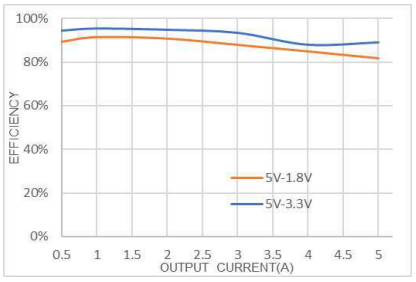
Typical Performance Characteristics (1)(2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): V_{IN} =5V, V_{OUT}=3.3V, T_A = +25ºC, C_{SS}=100nF, unless otherwise noted.

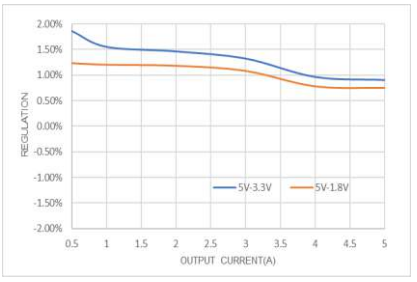
Efficiency vs Load Current

V_{OUT}=3.3V, 1.8V



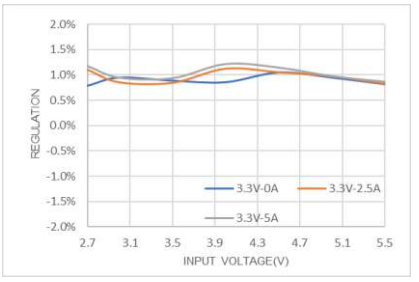
Load Regulation

V_{OUT}=3.3V, 1.8V



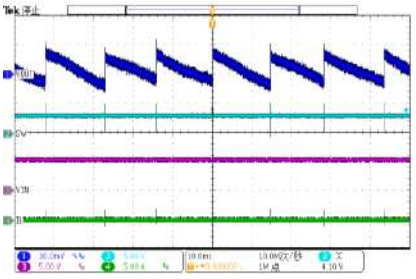
Line Regulation

V_{OUT}=3.3V



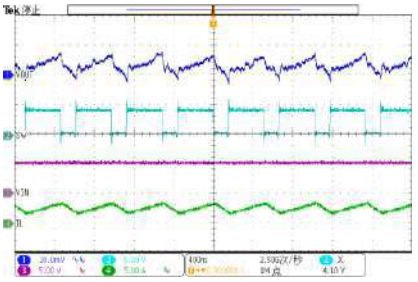
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A



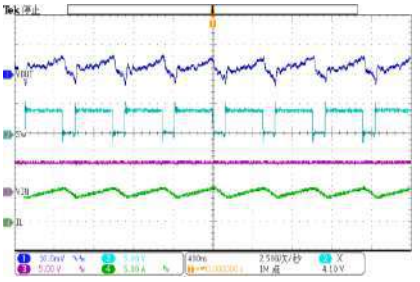
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=2.5A



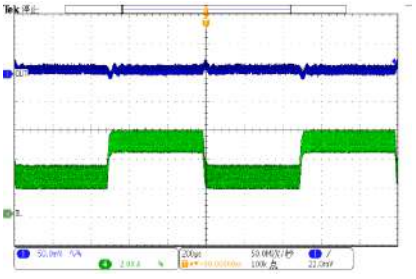
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=5A



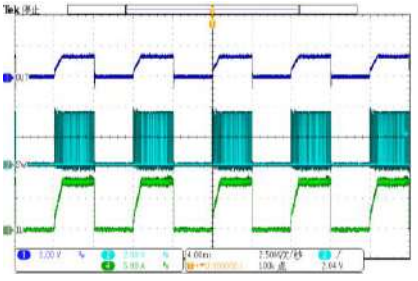
Loop Response

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=2.5A-5A



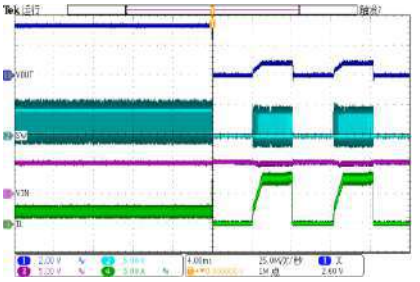
Output Short

V_{IN}=5V, V_{OUT}=3.3V



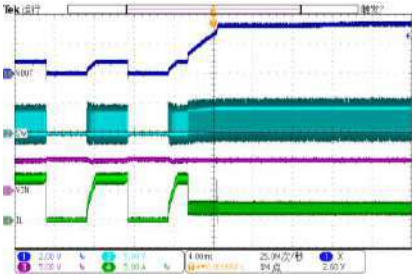
Short Circuit Entry

V_{IN}=5V, V_{OUT}=3.3V



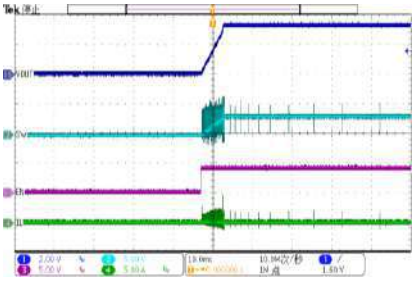
Short Circuit Recovery

V_{IN}=5V, V_{OUT}=3.3V



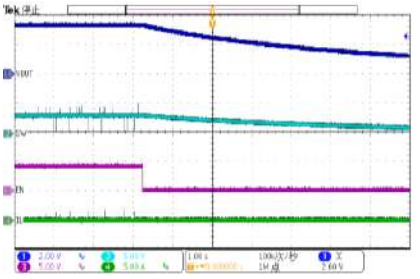
Enable Startup at No Load

V_{IN}=5V, V_{OUT}=3.3V



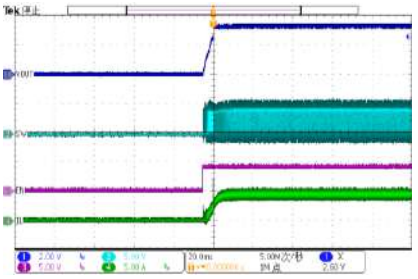
Enable Shutdown at No Load

V_{IN}=5V, V_{OUT}=3.3V



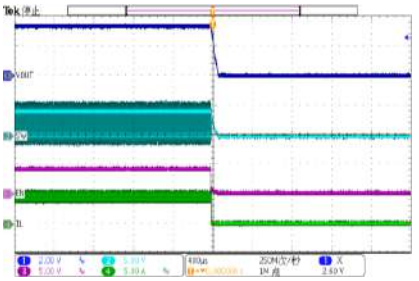
Enable Startup at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=5A



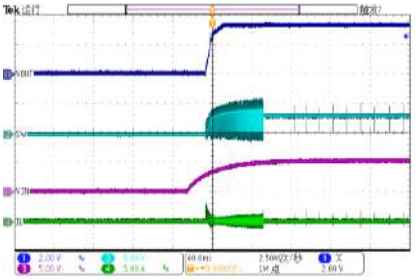
Enable Shutdown at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=5A



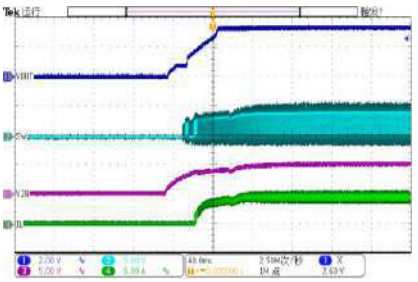
Power Up at No Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=0A

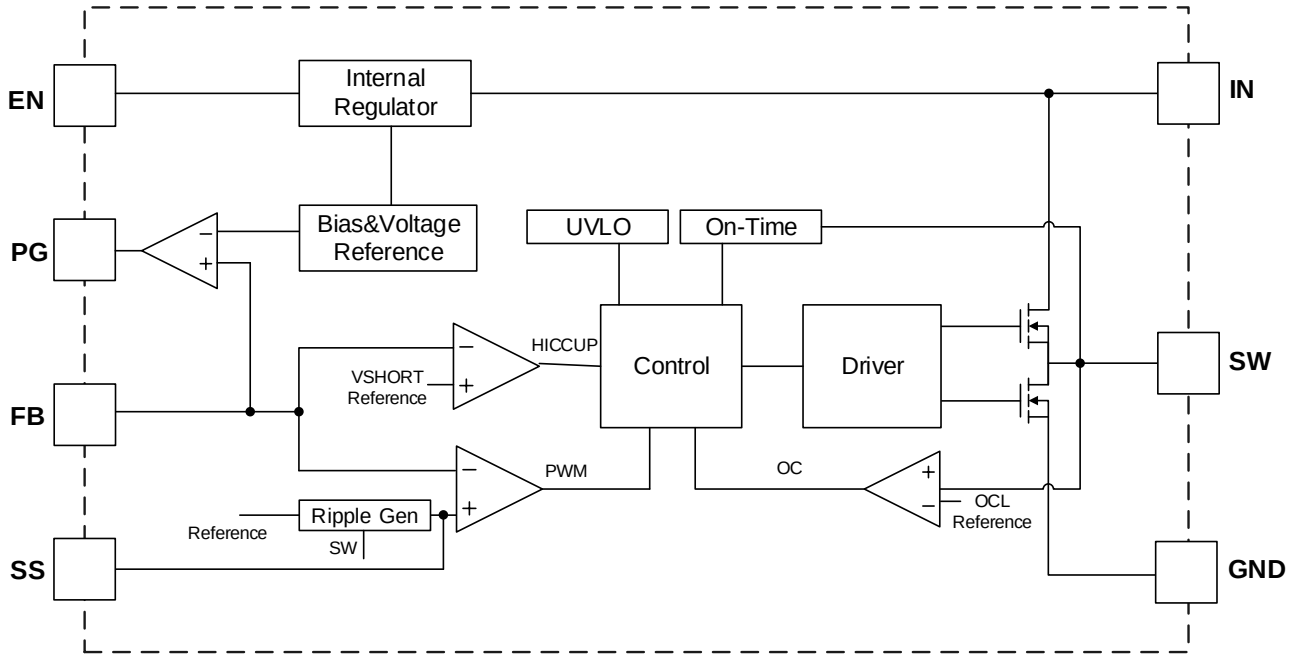


Power Up at Full Load

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=5A



Functional Block Diagram



ASP9050 Block Diagram

Functions Description

Operation

The ASP9050 uses a constant on time, ECOT mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, ICOMP, resets the RS latch. The peak inductor current at which ICOMP resets the RS latch, is controlled by the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage, FB, relative to the 0.6V reference, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator IRCMP, or the beginning of the next clock cycle.

PG (Power Good)

The power good is an open-drain output. Connect an above 100k pull up resistor to VIN to obtain an output voltage. When the FB pin is between 95% and 104% of internal voltage reference the PG, pin is pulled high. The PG pin is pulled low when FB is lower than 91% or higher than 108%of normal internal reference voltage.

SS (Power Start)

The ASP9050 provides an external soft-start pin that gradually raises the output voltage. The soft-start time can be programed by the external capacitor between SS pin and GND. The chip provides a 10uA charge current for the external capacitor. If a 0.1uF capacitor is used to set the soft-start and its period will be 6ms. If set this to NC, the soft-start time will be 0.6ms. The calculations for the slow-start time and slow-start capacitor are shown in the next equation:

$$Tss = \frac{C_{SS} \times V_{REF}}{I_{SS}}$$

Enable Operation

Pulling the EN pin low (<0.8V) will shut down the device. During shut mode, the ASP9050 shutdown current drops to lower than 0.1uA, Driving the EN pin high (>1.4V) will turn on the IC again.

Applications Information

Setting the Output Voltage

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

When sizing R2, in order to achieve low current consumption and acceptable noise sensitivity, use a maximum of 200kΩ for R2. Larger currents through R2 improve noise sensitivity and output voltage accuracy but increase current consumption.

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	R_{PG}(KΩ)	R_{SVIN}(Ω)	L1(μH)	C_{IN}(μF)	C_{OUT}(μF)	C_{SS}(nF))	C_{FF} (pF) Opt.
0.9	50	100	100	10	0.27	22×2	22×4	100	C_{FF} Chapter
1.0	66.67	100	100	10	0.33	22×2	22×4	100	C_{FF} Chapter
1.2	100.00	100	100	10	0.33	22×2	22×4	100	C_{FF} Chapter
1.5	150.00	100	100	10	0.47	22×2	22×4	100	C_{FF} Chapter
1.8	200.00	100	100	10	0.47	22×2	22×4	100	C_{FF} Chapter
2.5	316.67	100	100	10	0.47	22×2	22×4	100	C_{FF} Chapter
3.3	450.00	100	100	10	0.47	22×2	22×4	100	C_{FF} Chapter

All the external components are the suggested values, the final values are based on the application testing results.

Inductor Selection

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the maximum inductor peak current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. The inductor value can be calculated with:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% to 40% of the maximum load current. The maximum inductor peak current can be estimated as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency. Larger inductances lead to smaller ripple currents and voltages, but they also have larger physical dimensions, lower saturation currents and higher linear impedance. Therefore, the choice of inductance should be compromised according to the specific application.

Input Capacitor Selection

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. For a better performance, use ceramic capacitors placed as close to VIN as possible and a 0.1μF input capacitor to filter out high frequency interference is recommended. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

From the above equation, it can be concluded that the input ripple current reaches its maximum at V_{IN}=2V_{OUT} where $I_{CIN} = \frac{I_{OUT}}{2}$. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimate with Equation:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Similarly, when V_{IN}=2V_{OUT}, input voltage ripple reaches its maximum of $\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$.

Selecting the Output Capacitor

Because the ASP9050's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, VIN. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at VIN, large enough to damage the part. When choosing the input and output ceramic capacitors, choose the X5R or X7R

dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

A larger output capacitor can achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value (C_{OUT_MAX}) can be limited approximately with Equation:

$$C_{OUT\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{SS}/V_{OUT}$$

Where L_{LIM_AVG} is the average start-up current during the soft-start period, and T_{SS} is the soft- start time.

On the other hand, special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

Feed-Forward Capacitor (C_{FF})

ASP9050 has internal loop compensation, so adding C_{FF} is optional. Specifically, for specific applications, if necessary, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (C_{FF}) in the feedback network is to improve the transient response or higher phase margin. For optimizing the feed-forward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feed-forward capacitor identified, the value of feed-forward capacitor (C_{FF}) can be calculated with the following equation:

$$C_{FF} = \frac{1}{2\pi \times F_{CROSS}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

Where F_{CROSS} is the cross frequency.

To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

PC Board Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the VIN Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. VOUT, LX away from sensitive analog areas such as FB.
5. Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

Ordering and Marking Information

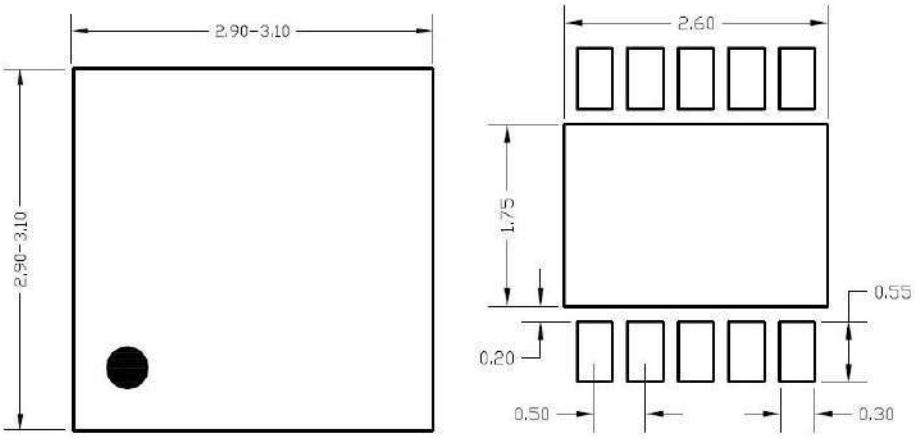
Ordering Device No.	Marking	Package	Packing	Quantity
ASP9050TI-R	AREAA	DFN3*3-10	Tape&Reel	3000/Reel

Top Marking:AREAA(device code:AR,E=year code,AA=lot number code)

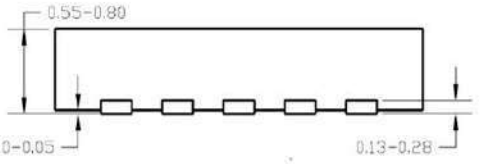
PACKAGE	MARKING
DFN3*3-10	AREAA

Package Description

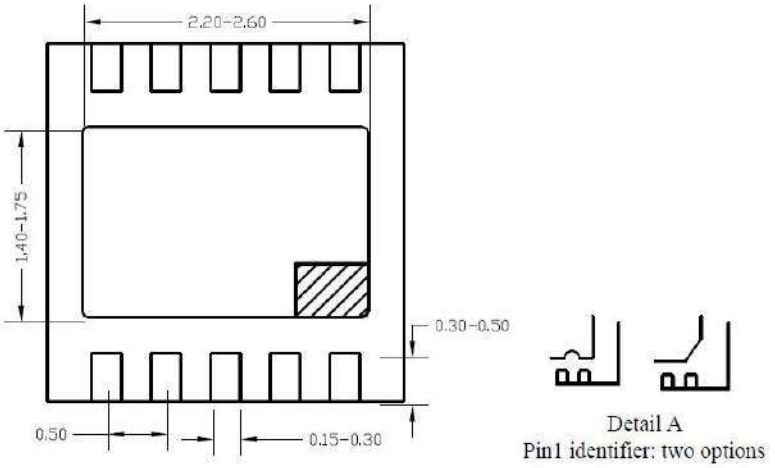
DFN3*3-10



TOP VIEW　　RECOMMENDED PAD LAYOUT



SIDE VIEW



BOTTOM VIEW

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

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