500mA High PSRR, Low Noise, Low Power LDO

Features

- Input Voltage Range: 2V to 5.5V
- Output Voltage Range: 1.1V to 4.5V
- Output Voltage Tolerance: ±2%
- Low Shutdown Current: 0.1μA (Typ.)
- Low Power Consumption: 28μA (Typ.)
- Low Dropout: 0.15V@100mA
- High PSRR: 70dB@1KHz (Typ.)
- Over Current Protection
- Short Circuit Protection
- Thermal Shutdown Protection
- –40°C to 125°C Operating Junction Temperature
- SOT23-5/ SOT23-3/DFN4-1×1 Package

Applications

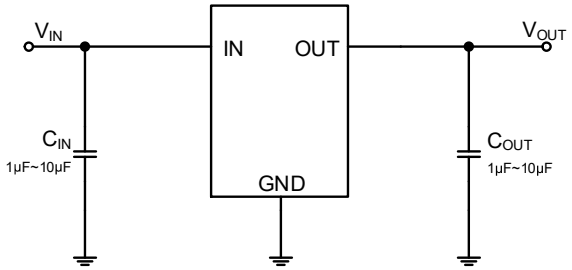
- Mobile Phones, Tablets
- Portable Medical Equipment
- IP Cameras
- Digital Cameras and Audio Devices
- Portable and Battery-Powered Equipment
- Drones

General Description

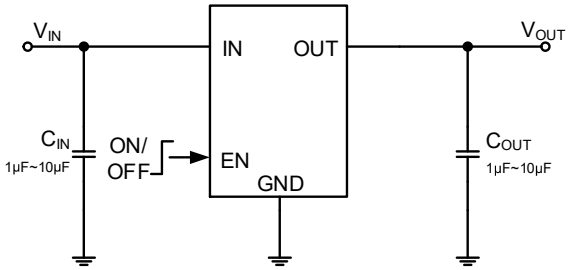
The ASPL6050G series are highly accurate, low noise, CMOS LDO Voltage Regulators. Offering low output noise, high ripple rejection ratio, low dropout and very fast turn-on times. The ASPL6050G's current limiters' feedback circuit also operates as a short protect for the output current limiter and the output pin. The output voltage is set by current trimming. Voltages are selectable in 50mV steps within a range of 1.1V to 4.5V.

The ASPL6050G series is also fully compatible with low ESR ceramic capacitors, reducing cost and improving output stability. This high level of output stability is maintained even during frequent load fluctuations, due to the excellent transient response performance and high PSRR achieved across a broad range of frequencies. The EN function allows the output of regulator to be turned off, resulting in greatly reduced power consumption. The ASPL6050G series are available in SOT23-3, SOT23-5, DFN4-1×1 package.

Typical Application Circuit



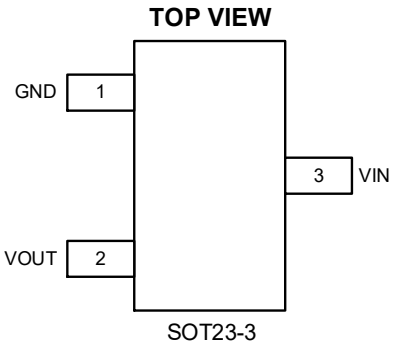
SOT23-3 Typical Application Circuit



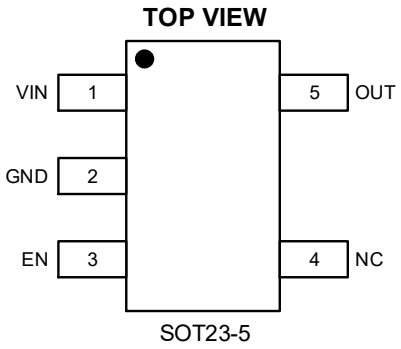
SOT23-5/DFN1×1-4 Typical Application Circuit

Pin Description

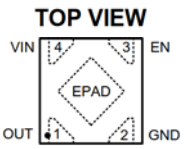
Pin Configuration



SOT23-3



SOT23-5



DFN1×1-4

Pin Description

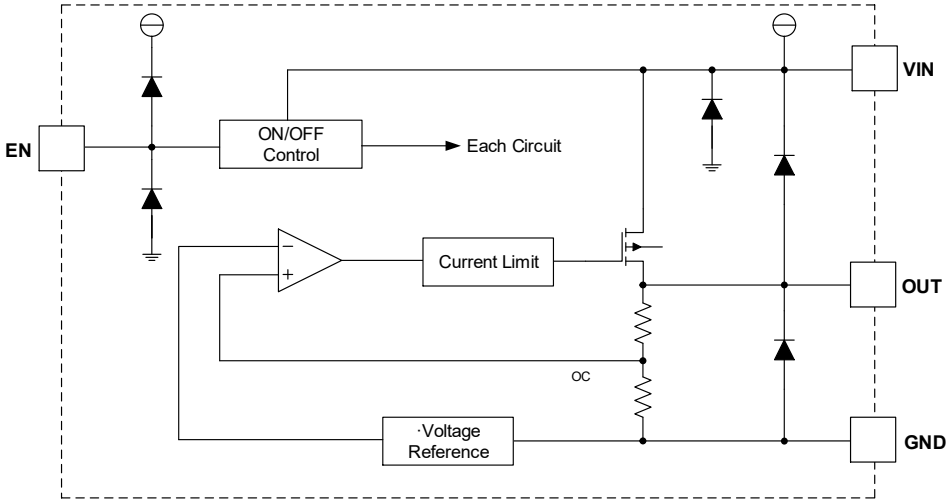
SOT23-3 Pin No.	SOT23-5 Pin No.	DFN1×1-4 Pin No.	Pin Name	Function
3	1	4	VIN	Input voltage pin for the regulator.
1	2	2	GND	Ground pin.
-	3	3	EN	Enable Control (Active high), Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
-	4	-	NC	Not Connected.
2	5	1	OUT	Output voltage pin for the regulator.
-	-	EPAD	EPAD	Exposed pad should be connected directly to the GND pin.

Ordering Information

Ordering Device No.	Package	Packing	Quantity
ASPL6050G-XXZB-R	SOT23-3	Tape&Reel	3000/Reel
ASPL6050G-XXZD-R	SOT23-5	Tape&Reel	3000/Reel
ASPL6050G-XXTG-R	DFN1x1-4	Tape&Reel	5000/Reel

Note: ”G” stands for fixed output voltage series.
Note: ”XX” stands for Output Voltage. "11": 1.1V, "12": 1.2V, "15": 1.5V, "18": 1.8V, "25": 2.5V, "28": 2.8V, "30": 3.0V, "33": 3.3V, "36": 3.6V, "38": 3.8V, "40": 4.0V, "42": 4.2V.
Note: ”ZB, ZD, TG” stands for package. "ZB": SOT23-3, "ZD": SOT23-5, "TG": DFN1x1-4.
Note: ”R” stands for Packing, Tape&Reel.
P/N example: ASPL6050G-18ZB-R, ASPL6050G-25ZB-R, ASPL6050G-33ZB-R, ASPL6050G-18TG-R, etc.

Functional Block Diagram



Functional Block Diagram

Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V_{IN} voltage	2	6	V
V_{OUT} voltage	1	5	V
Output Current (3)	500		mA
Power dissipation (4)	Internally Limited		
Operating Ambient Temperature	-40	85	°C
Maximum junction temperature		150	°C
Storage temperature, T_{stg}	–50	85	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): $I_{OUT}=P_D/(V_{IN}-V_{OUT})$

Note (4): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=155°C (typical) and disengages at T_J= 140°C (typical).

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	2	5.5	V
Output current	0	500	mA

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	SOT23 3 Pin	SOT23 5 Pin	DFN1×1 4 Pin	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	208	195	216	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	112	102	161	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56	46	162	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	8.5	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52	45	162	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	123	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1)

T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions			Min	Typ.	Max	Units
Input Voltage	V_{IN}				2		5.5	V
Output Voltage	V_{OUT}	V_{IN}=V_{OUT}+1V I_{OUT}=1mA to 500mA			V_{OUT}×0.98		V_{OUT}×1.02	V
Output Current	I_{OUT}	V_{IN}≥$V_{OUT(S)}$+1.0V				500		mA
Output Current Limit	I_{CL}	V_{IN}=5V, 1.8V<V_{OUT}<3.3V			450	500	550	mA
Dropout Voltage V_{OUT}=0.98V_{OUT} (NOM)	V_{drop}	-40°C ≤ T_J ≤ 125°C	3.3V	100mA		60		mV
				300mA		230		
			2.5V	100mA		70		
				300mA		250		
			1.2V	100mA		430		
				300mA		700		
Line Regulations	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$	$V_{OUT(S)}$+0.5 V≤V_{IN}≤7V I_{OUT}=300mA			-	0.20	0.60	%/V
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	V_{IN}=$V_{OUT(S)}$+1.0 V			-	0.50	2	%
Supply current	I_{SS1}	V_{IN}=$V_{OUT(S)}$+1.0 V			-	28		μA
Shutdown Current	I_{SD}	V_{EN}=0.3V (Disable)				0.1		μA
Power Supply Rejection Ratio	PSRR	V_{OUT}=2.5V,	f = 1KHz		-	70	-	dB
		I_{OUT}=20mA	f = 10kHz			60	-	dB
Short-Circuit Current Limit	I_{SC}					500	-	mA
High Input Threshold	V_{ENH}	VEN rising until the output is enabled			0.9			V
Low Input Threshold	V_{ENL}	VEN falling until the output is disabled					0.4	V
Input Current at EN pin	I_{EN}	V_{IN}=V_{EN}=$V_{OUT(T)}$+1V			-0.1		0.1	μA
		V_{IN}=$V_{OUT(T)}$+1V, V_{EN}=V_{SS}			-0.1		0.1	μA
Thermal Shutdown Temperature	T_{SD}	T_J rising				155		°C
Thermal Shutdown Hysteresis	ΔT_{SD}	T_J falling from shutdown				15		°C

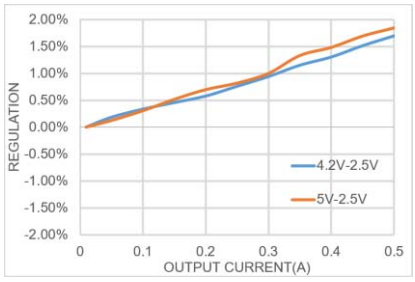
Note (1): All of specification is verified by design.

Typical Performance Characteristics (1)

Note (1): Typical performance characteristics below based on T_A = 25°C, unless otherwise noted.

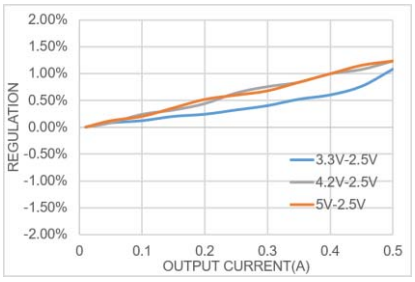
Load Regulation

V_{OUT}=3.3V



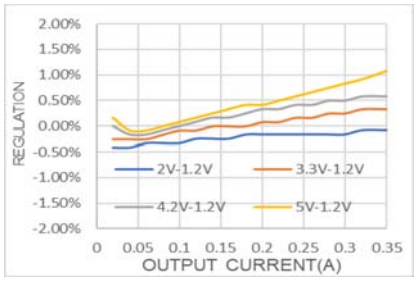
Load Regulation

V_{OUT}= 2.5V



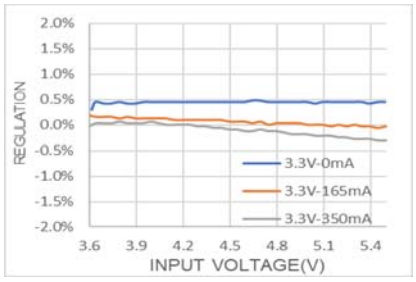
Load Regulation

V_{OUT}=1.2V



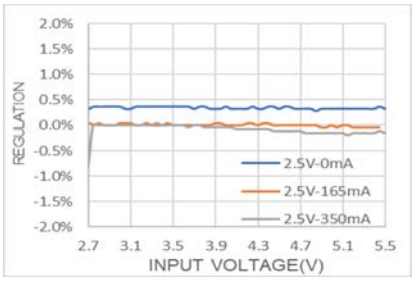
Line Regulation

V_{OUT}=3.3V



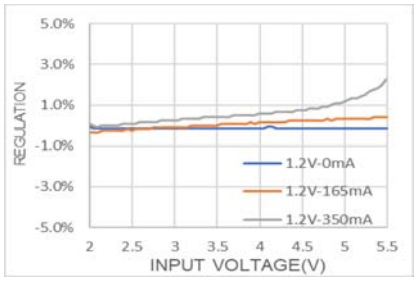
Line Regulation

V_{OUT}=2.5V



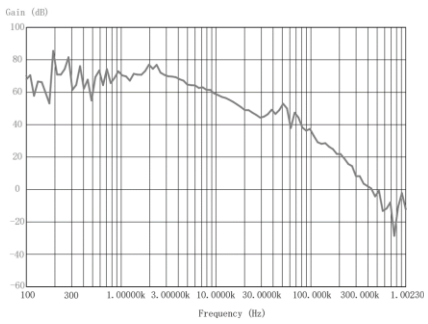
Line Regulation

V_{OUT}=1.2V



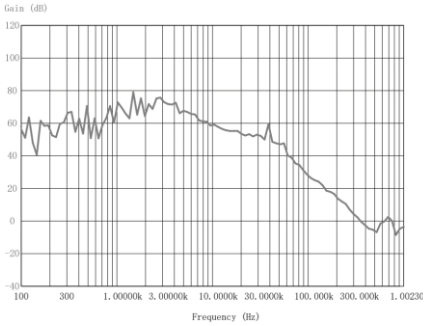
Power Supply Rejection Ration

V_{IN}=3.3V, V_{OUT}=1.2V, I_{OUT}=20mA



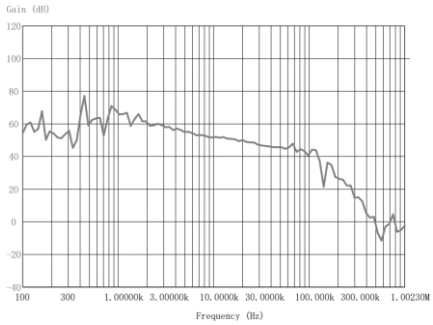
Power Supply Rejection Ration

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=20mA



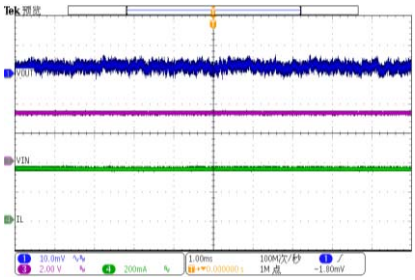
Power Supply Rejection Ration

V_{IN}=5V, V_{OUT}=3.3V, I_{OUT}=20mA



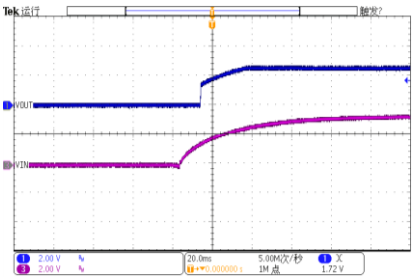
Steady State

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=350mA



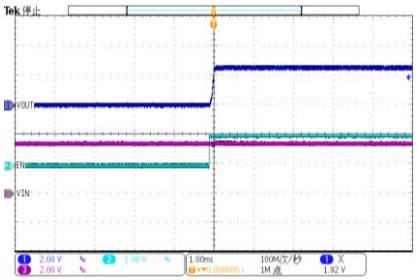
Vin Start Up

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=1mA



EN Start Up

V_{IN}=3.3V, V_{OUT}=2.5V, I_{OUT}=1mA



Applications Information

Internal Current Limit and Short-Circuit Protection

The ASPL6050G series includes a combination of a fixed current limiter circuit & a feedback circuit, which aid the operations of the current limiter and circuit protection. When the load current reaches the current limit level, the fixed current limiter circuit operates and output voltage drops. As a result of this drop-in output voltage, the feedback circuit operates, output voltage drops further and output current decreases.

Thermal Shutdown Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating. The thermal shutdown circuitry of the ASPL6050G has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the ASPL6050G device into thermal shutdown may degrade device reliability.

Enable (EN pin)

The EN pin voltage must be higher than the V_{ENH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{ENL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

Layout Guidelines

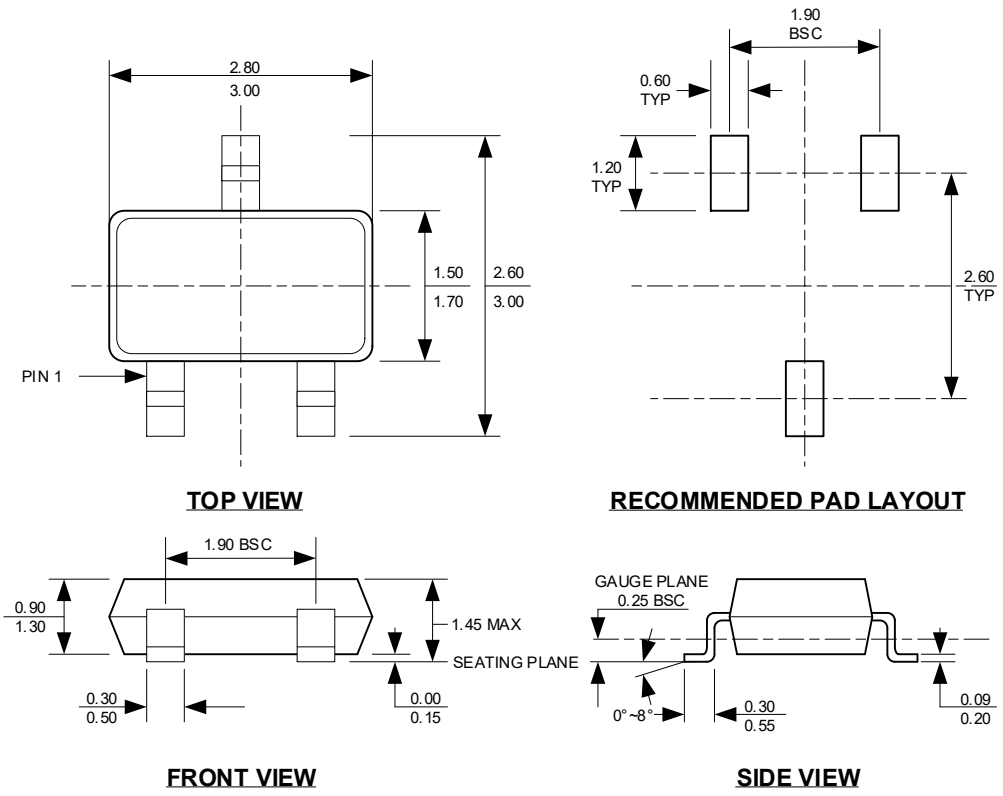
The dynamic performance of the ASPL6050G is dependent on the layout of the PCB.

1. Best performance is achieved by placing C_{IN} and C_{OUT} as close to the IC as possible.
2. The ground connections for C_{IN} and C_{OUT} must be back to the IC's GND pin using as wide and short a copper trace as is practical.
3. Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

Packaging Information

3-Pin SOT23 Outline Dimensions

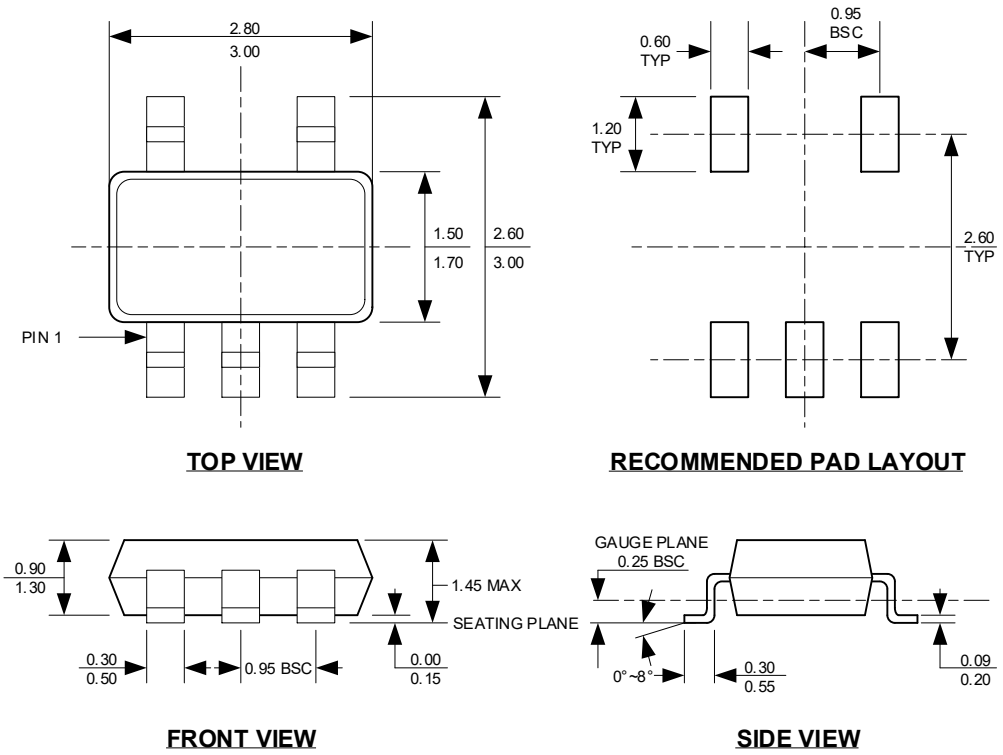
SOT23-3



NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

5-Pin SOT23 Packaging Information

SOT23-5



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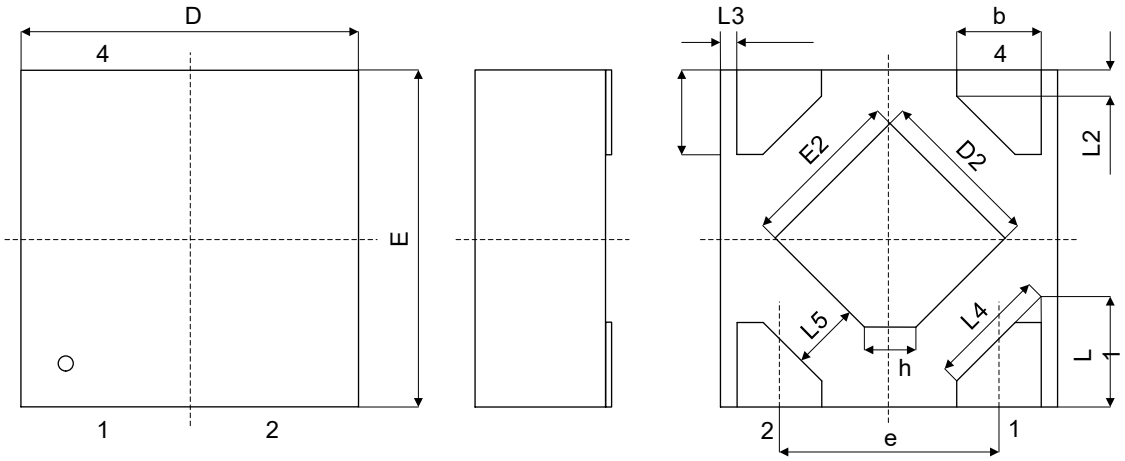
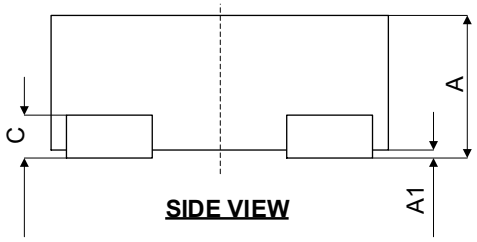
6. DRAWING IS NOT TO SCALE.

4-Pin DFN1×1 Packaging Information

DFN1x1-4





DIM / Symbol	Min (mm)	Nom (mm)	Max (mm)
A	0.35	-	0.40
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.02	0.07	0.17
D	0.95	1.00	1.05
D2	0.38	0.48	0.58
e	0.65BSC		
E	0.95	1.00	1.05
E2	0.38	0.48	0.58
L	0.20	0.25	0.30
L2	0.077REF		
L3	0.05REF		
L4	0.34REF		
L5	0.20REF		
h	0.12REF		

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6. DRAWING IS NOT TO SCALE.

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