■ General Description

The ASPS6601 is an integrated power switch for self-powered and bus-powered Universal Serial Bus (USB) application. The ASPS6601 has several protections features such as current limiting and thermal shutdown to prevent catastrophic switch failure caused by increasing power dissipation when continuous heavy loads or short circuit occurs. A built-in P-channel MOSFET used for power MOS has superior Ron and easy control characteristics. The output reverse-current protection turns off the MOSFET switch whenever occurs the unexpected continuously reverse current. ($\overline{FLAG}$) pin is an open-drain output report overcurrent or over-temperature event and has typical 8.5ms deglitch timeout period. ASPS6601 is available in SOT23-5, TSOT23-5, TSOT23-6,MSOP-8,DFN-6(2x2x0.75mm) packages.

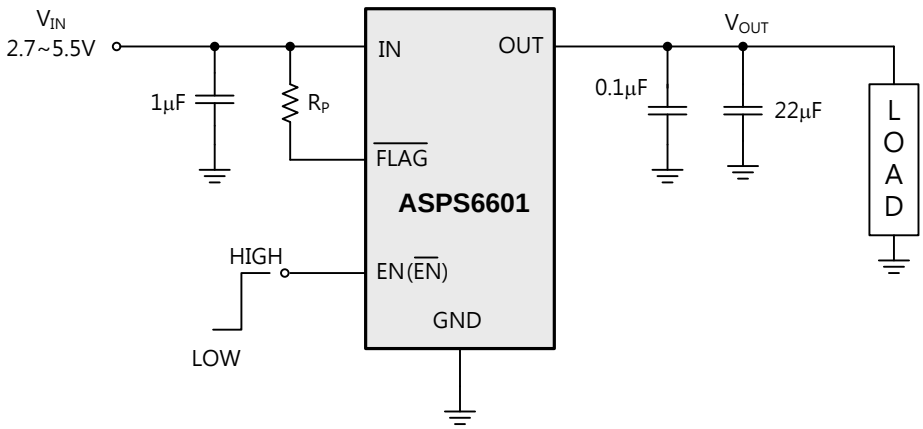
■ Features

- Operating Range: 2.7V to 5.5V
- 55mΩ(Typ.) High-Side MOSFET
- Constant Current during Over-Current and Current Limit with Fold-Back are Available
- Active High or Active Low Version is Available
- 1.6ms Rise Time at V_{IN} = 3.3V Condition
- Fast Short-Circuit Response : 1.5μS(Typ.)
- Under Voltage Lockout, Over-Current, Output-Voltage and Thermal Protection
- Deglitched Open-Drain Flag Output ($\overline{FLAG}$)

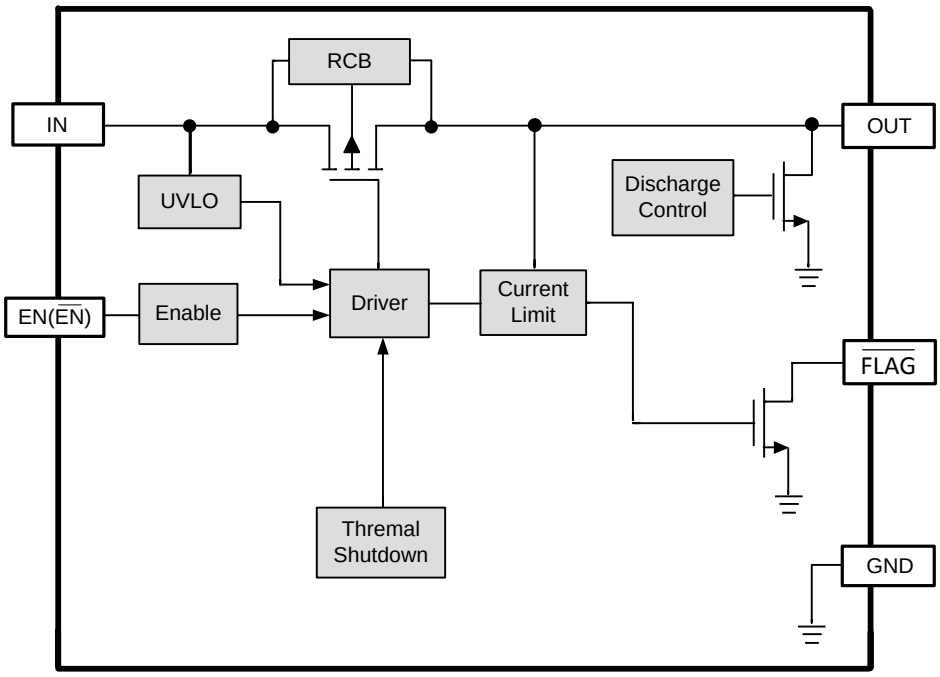
■ Application

- Laptops, Desktops, AIO
- Set-Top Boxes
- LCD TVs & Monitors
- Residential Gateways
- e-Readers, Printers, Hubs
- Docking, HUB

■ Typical Application Schematic



■ Function Block Diagram



■ Ordering Information

ASPS6601x-XXXxx-X-R

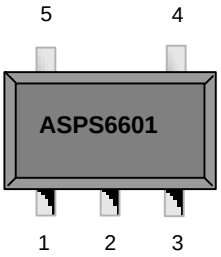
- **"X": Pin Configuration**
- **"xx": Package Type**
- **"XXX": Current Limit**
- **"x": Enable**

Note1: "x" is EN Pin funtion. A: Active High, B: Active Low.
Note2: "XXX" stands for Current Limit. Example: "200"=2.0A, "250"=2.5A, "300"=3.0A, "340"=3.4A.
Note3: "xx" stands for package. "ZD"=SOT23-5, "ZE"=TSOT23-5, "ZF"=TSOT23-6, "N6"=DFN6, "MS"=MSOP-8.
Note4: "X" stands for Pin Configuration, A, B, C, please refer to Pin Configuration.
Note5: "R" stands for Packing, Tape&Reel.

P/N example: ASPS6601A-200ZD-A-R, ASPS6601B-200ZF-A-R, ASPS6601A-340N6-R, etc.

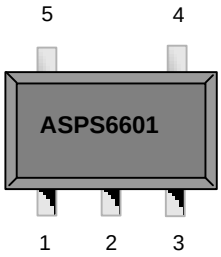
■ Pin Configuration

SOT23-5
Top View



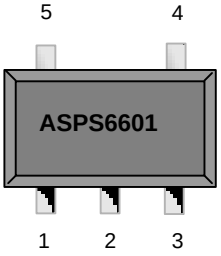
ASPS6601x-XXXZD-A
1. OUT
2. GND
3. FLAG
4. EN(EN)
5. IN

SOT23-5
Top View



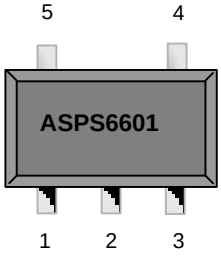
ASPS6601x-XXXZD-B
1. EN(EN)
2. GND
3. FLAG
4. IN
5. OUT

SOT23-5
Top View



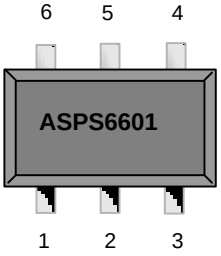
ASPS6601x-XXXZD-C
1. FLAG
2. GND
3. EN(EN)
4. IN
5. OUT

TSOT23-5
Top View



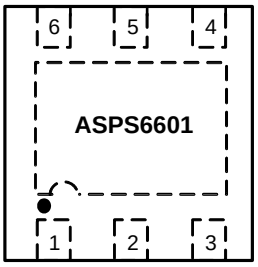
ASPS6601x-XXXZE-A
1. OUT
2. GND
3. FLAG
4. EN(EN)
5. IN

TSOT23-6
Top View



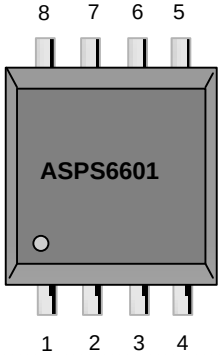
ASPS6601x-XXXZF-A
1. OUT
2. GND
3. FLAG
4. EN(EN)
5. NC
6. IN

DFN-6
(2x2x0.75mm)
Top View



ASPS6601x-XXXN6
1. IN
2. GND
3. EN(EN)
4. FLAG
5. OUT
6. NC

MSOP-8
Top View



ASPS6601x-XXXMS
1. GND
2. IN
3. IN
4. EN(EN)
5. FLAG
6. OUT
7. OUT
8. OUT

■ Pin Description

Pin Name	I/O	Description	Pin Number			
			SOT23-5			TSOT23-5
			A	B	C	A
IN	I	Input Voltage; Place a 1μF or greater ceramic capacitor from IN to GND as close as possible to the IC.	5	4	4	5
GND	NA	Ground connection.	2	2	2	2
OUT	O	Power-switch output.	1	5	5	1
EN	I	Enable input; logic high turns on power switch.	4	1	3	4
$\overline{EN}$	I	Enable input; logic low turns on power switch.	4	1	3	4
$\overline{FLAG}$	O	Active-low open-drain output, asserted during over current, over temperature or reverse voltage conditions. Connect a 10kΩ or greater resistor pull-up, otherwise floating.	3	3	1	3

Pin Name	I/O	Description	Pin Number		
			TSOT23-6	DFN-6	MSOP8
			A		
IN	I	Input Voltage; Place a 1μF or greater ceramic capacitor from IN to GND as close as possible to the IC.	6	1	2, 3
GND	NA	Ground connection.	2	2	1
OUT	O	Power-switch output.	1	5	6, 7, 8
EN	I	Enable input; logic high turns on power switch.	4	3	4
$\overline{EN}$	I	Enable input; logic low turns on power switch.	4	3	4
$\overline{FLAG}$	O	Active-low open-drain output, asserted during over current, over temperature or reverse voltage conditions. Connect a 10kΩ or greater resistor pull-up, otherwise floating.	3	4	5
NC	NA	No Connection	5	6	NA

■ Absolute Maximum Ratings

Parameter		Value	Unit
Input Voltage		-0.3 to 6.0	V
Enable Voltage		-0.3 to 6.0	V
Output Voltage		-0.3 to 6.0	V
$\overline{FLAG}$ Voltage		-0.3 to 6.0	V
ESD Ratings	HBM	±4000	V
	MM	±200	V
	CDM	±1000	V
	IEC 61000-4-2 Contact Discharge	±8000	V
	IEC 61000-4-2 Air-gap Discharge	±15000	V

■ Recommended Operation Conditions

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	2.7 to 5.5	V
Ambient Temperature Range	T_A	-40 to +85	°C
Junction Temperature Range	T_J	-40 to +125	
Storage Temperature	T_{STG}	-60 to +150	

Part Number	Continuous Load Current	Typical Current Limit
ASPS6601x-200XX	1.5A	2.0A
ASPS6601x-250XX	2.0A	2.5A
ASPS6601x-300XX	2.5A	3.0A
ASPS6601x-340XX	3.0A	3.4A

■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	SOT23-5	Conductive Epoxy	θ_{JC}	81	°C / W
	TSOT23-5			81	
	TSOT23-6			81	
	DFN-6			16	
	MSOP-8			80	
Thermal Resistance (Junction to Ambient)	SOT23-5	Conductive Epoxy	θ_{JA}	260	°C / W
	TSOT23-5			260	
	TSOT23-6			260	
	DFN-6			66	
	MSOP-8			206	
Internal Power Dissipation	SOT23-5	Conductive Epoxy	P_D	400	mW
	TSOT23-5			400	
	TSOT23-6			400	
	DFN-6			1515	
	MSOP-8			625	
Lead Temperature (soldering 10 sec)**				300	°C

* Measure θ_{jc} on top of package.

** MIL-STD-202G 210F

■ Electrical Specifications

V_{IN} = 5V, C_{IN} = 1μF, C_{OUT} = 22μF, R_L = 10Ω, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Test Condition		Min	Typ	Max	Units
Input Voltage	V_{IN}			2.7		5.5	V
Quiescent Current	I_Q	V_{IN} = 5V, Enabled, OUT = Open			65	100	μA
Shutdown Current	I_{SHDN}	V_{IN} = 5.5V , Disabled			1	1.5	μA
Input UVLO	V_{UVLO}	V_{IN} Rising		2	2.4	2.6	V
Switch On-Resistance	$R_{DS(ON)}$	V_{IN} = 5.0V			55	85	mΩ
Current Limit	I_{LIM}	V_{IN} = 5V, V_{OUT} = 4.5V	ASPS6601x-200XX	1.8	2.0	2.2	A
			ASPS6601x-250XX	2.25	2.5	2.75	
			ASPS6601x-300XX	2.7	3	3.3	
			ASPS6601x-340XX	3.1	3.4	4.0	
Short-Circuit Current Limit	I_{Short}	OUT Connected to GND	ASPS6601x-200XX		0.5		A
			ASPS6601x-250XX		0.625		
			ASPS6601x-300XX		0.75		
			ASPS6601x-340XX		0.875		
EN Input Threshold -High	V_{IH}	V_{IN} = 2.7V to 5.5V		1.2			V
EN Input Threshold -Low	V_{IL}	V_{IN} = 2.7V to 5.5V				0.6	
Output Turn-On Rise Time	t_R	V_{IN} = 3.3V, C_L = 1μF, R_{LOAD} = 100Ω		1.0	1.6	3	ms
		V_{IN} = 5V, C_L = 1μF, R_{LOAD} = 100Ω		1.5	2.2	4	
$\overline{FLAG}$ Blanking Time	t_{Blank}	Assertion and de-assertion due to overcurrent and over-temperature condition		5.6	8.5	10.5	ms
Response Time to Short Current	t_{IOS}	V_{IN} = 5V			1.5		μs
Reverse Current Limit	I_{ROCP}	V_{OUT} - V_{IN} = 150mV			0.4		A
Time from Reverse-Voltage Condition to MOSFET Turn Off	t_{TRIG}	V_{IN} = 5V		5.6	8.5	10.5	ms
Discharge Resistance	R_{DIS}	V_{IN} = 5V, Disabled, I_{OUT} = 1mA			150	235	Ω
Thermal Shutdown Threshold	T_{SHDN}				150		°C
Thermal Shutdown Hysteresis	T_{HYS}				25		°C

■ Application Information

Supply Filtering

A 1μF bypass capacitor from IN to GND, placed near the ASPS6601, is strongly recommended to control supply transients. Without a bypass capacitor, an output short may cause sufficient ringing on the input (from supply lead inductance) to damage internal control circuitry. Input transients must not exceed the absolute maximum supply voltage (V_{IN} max = 6V) even for a short duration.

ON and OFF Control

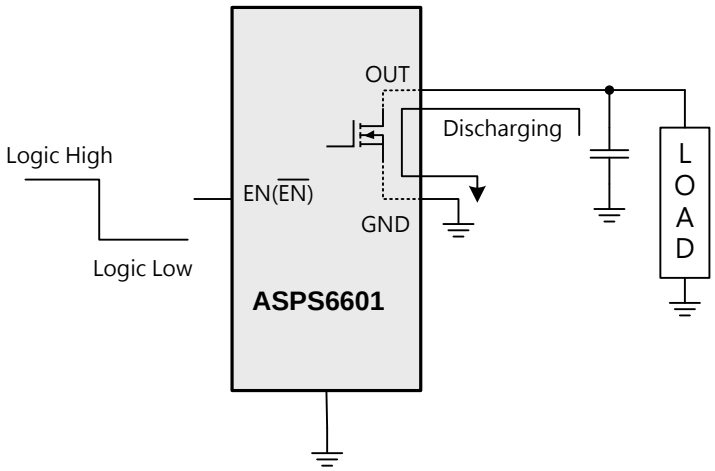
EN($\overline{EN}$) must be driven logic high or logic low for a clearly defined input. Floating the input may cause unpredictable operation. The pin should not be allowed to go negative with respect to GND.

Auto Output Discharge

The discharge function is activated when EN($\overline{EN}$) pin is disabled or de-asserted. The power switch automatically offers a resistive discharge path for the external storage capacitor. This facilitates discharging any residue of the output voltage when either no external output resistance or load resistance is present at the output.

EN	IN to OUT	OUT to GND
H	ON	OFF
L	OFF	ON

$\overline{EN}$	IN to OUT	OUT to GND
H	OFF	ON
L	ON	OFF



■ Application Information (Contd.)

$\overline{\text{FLAG}}$ Indicator

The $\overline{\text{FLAG}}$ open-drain output is asserted ($\overline{\text{FLAG}}$: active low) during an over-current or over-temperature condition. Until the fault condition is de-asserted and the ASPS6601 resumes normal operation. The ASPS6601 eliminate false $\overline{\text{FLAG}}$ reporting by using an internal delay "deglitch" circuit for over-current (8.5ms typ.) conditions without the need for external circuitry. This ensures that $\overline{\text{FLAG}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load.

Power Dissipation

Thermal analysis is strongly dependent on additional system level factors such as air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power.

Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the $R_{DS(ON)}$ of the internal MOSFET relative to the input voltage and operating temperature. As an initial estimate, make use of the highest operating ambient temperature of interest and read $R_{DS(ON)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times (I_{OUT})^2$$

Where:

P_D = Total power dissipation (W)

$R_{DS(ON)}$ = MOSFET on-resistance (Ω)

I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of internal MOSFET.

Next, the junction temperature of the device depends on different contributing factors such as board layout, ambient temperature, device environment, and so on. Then, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

T_A = Ambient temperature (°C)

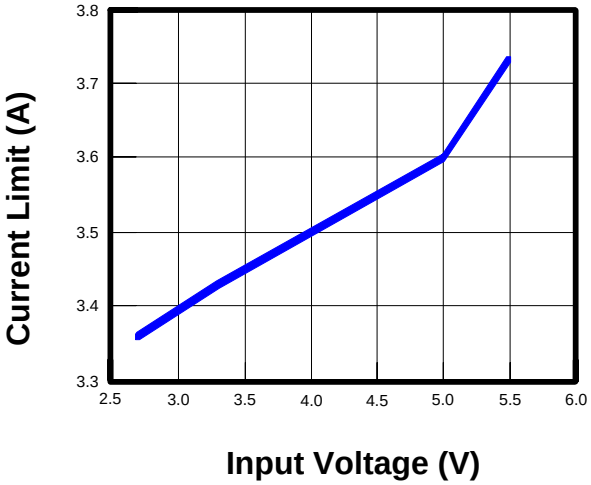
θ_{JA} = Thermal resistance (°C/W)

P_D = Total power dissipation (W)

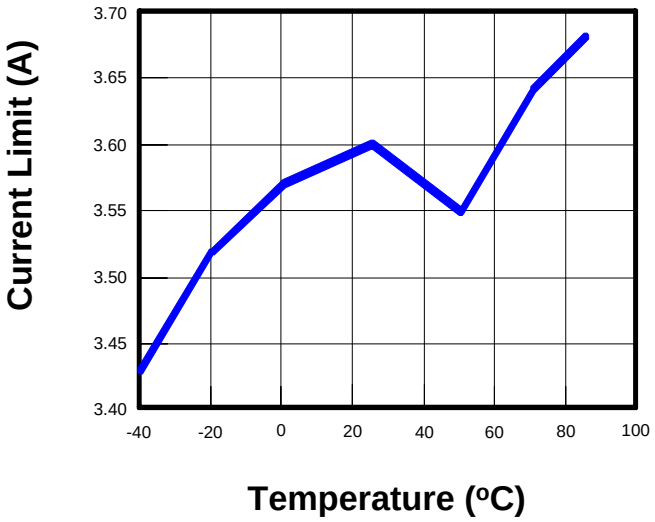
Compare the calculated T_J with the initial estimate. If they are not within a few degrees, repeat the calculation using the refined $R_{DS(ON)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final T_J is highly dependent on θ_{JA} and thermal resistance is respectably dependent on the individual package and board layout.

■ Characterization Curve

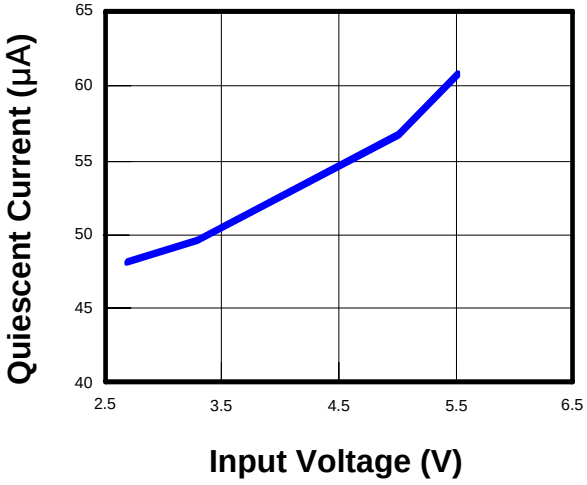
Current Limit vs. Input Voltage



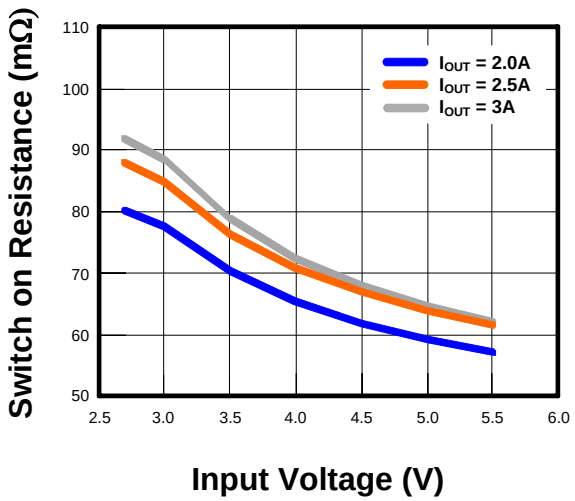
Current Limit vs. Temp



Quiescent Current vs. Input Voltage

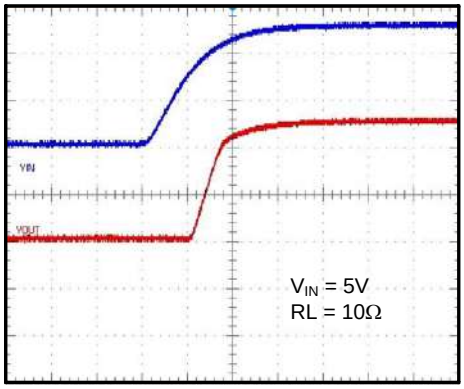


Switch on Resistance vs. Input Voltage



■ Characterization Curve (Contd.)

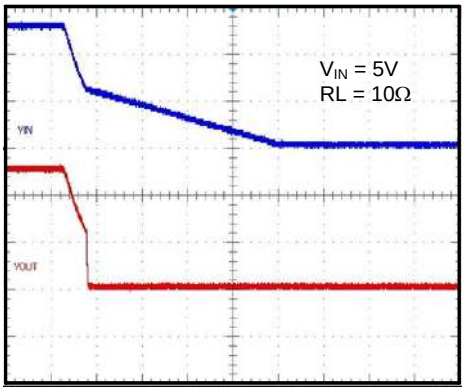
UVLO at Rising



Time (4.0ms / Div)

1. V_{IN} = 2V / Div
2. V_{OUT} = 2V / Div

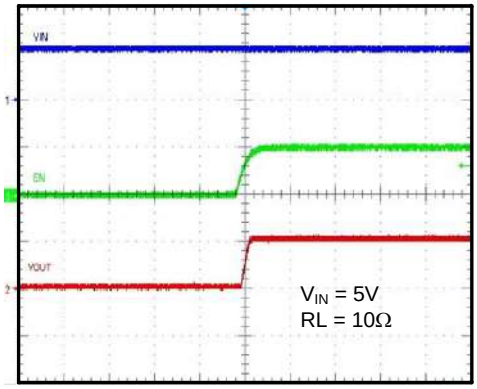
UVLO at Falling



Time (4.0ms / Div)

1. V_{IN} = 2V / Div
2. V_{OUT} = 2V / Div

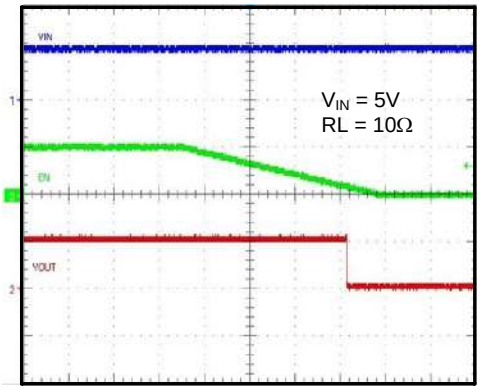
Turn on Delay Time and Rise Time



Time (20ms / Div)

1. V_{IN} = 5V / Div
2. V_{OUT} = 5V / Div
3. EN = 5V / Div

Turn off Delay Time and Fall Time

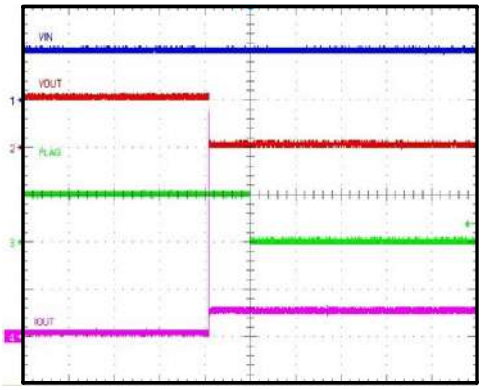


Time (20ms / Div)

1. V_{IN} = 5V / Div
2. V_{OUT} = 5V / Div
3. EN = 5V / Div

■ Characterization Curve (Contd.)

FLAG Response during Short Circuit

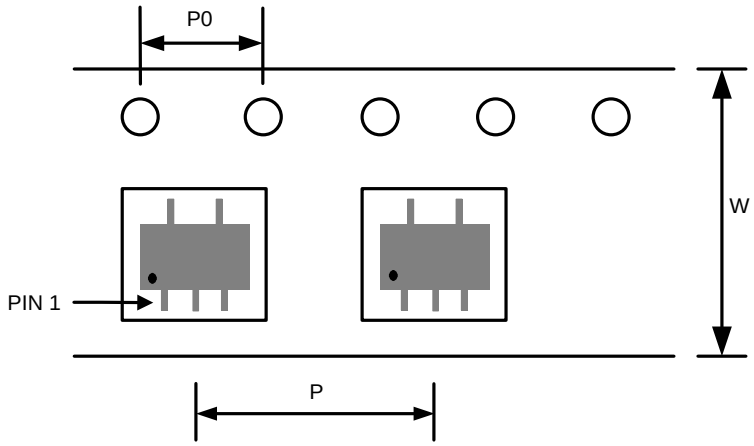


Time (10ms / Div)

1. V_{IN} = 5V / Div
2. V_{OUT} = 5V / Div
3. FLAG = 5V / Div
4. I_{OUT} = 1A / Div

■ Tape and Reel Dimension

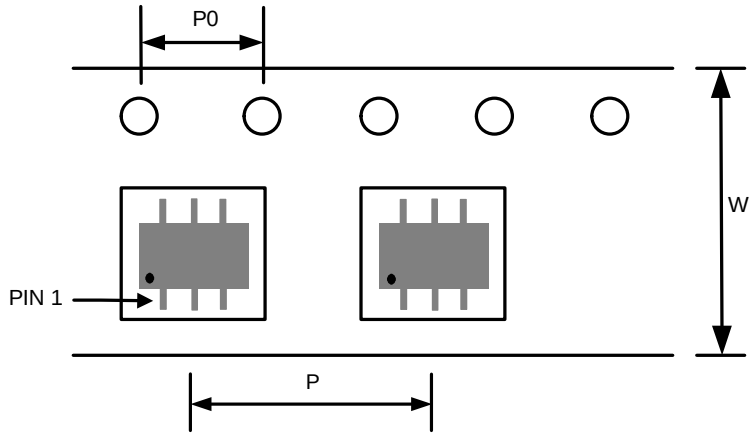
SOT23-5/TSOT23-5



Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
SOT23-5	8.0±0.1 mm	4.0±0.1 mm	4.0±0.1 mm	3000pcs	180±1 mm

TSOT23-6

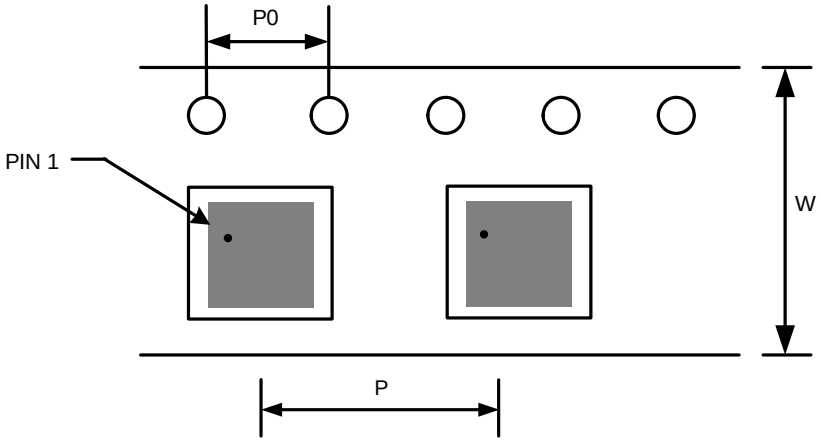


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
TSOT23-6	8.0±0.1 mm	4.0±0.1 mm	4.0±0.1 mm	3000pcs	180±1 mm

■ Tape and Reel Dimension (Contd.)

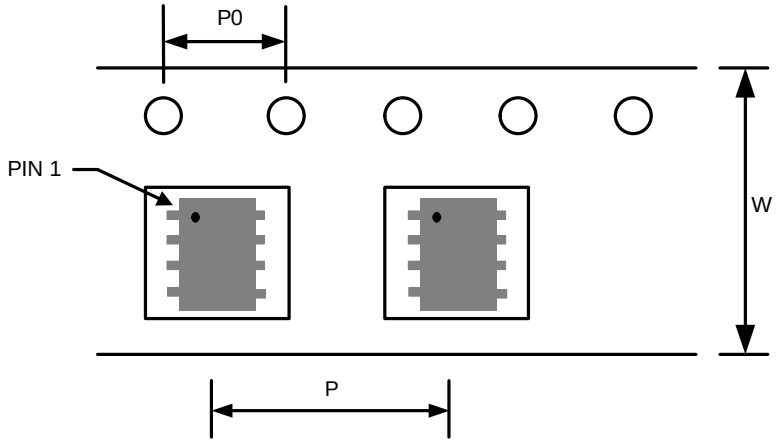
DFN-6
(2x2x0.75mm)



Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
DFN-6	8.0±0.1 mm	4.0±0.1 mm	4.0±0.1 mm	3000pcs	180±1 mm

MSOP-8

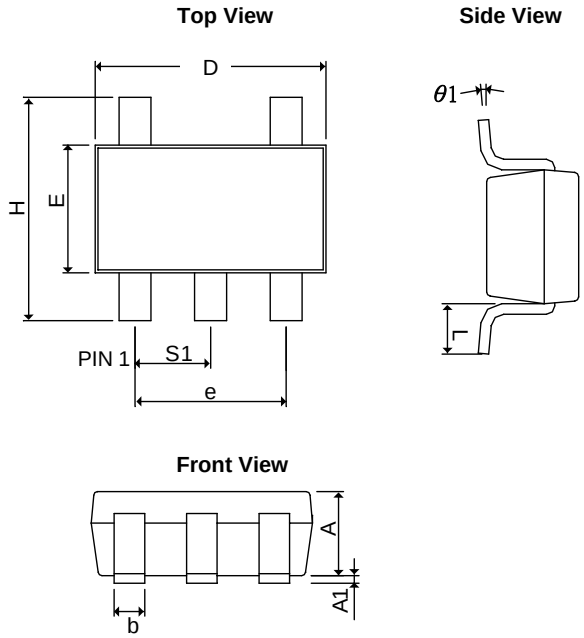


Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Pitch (P0)	Part Per Full Reel	Reel Size
MSOP-8	12.0±0.1 mm	8.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm

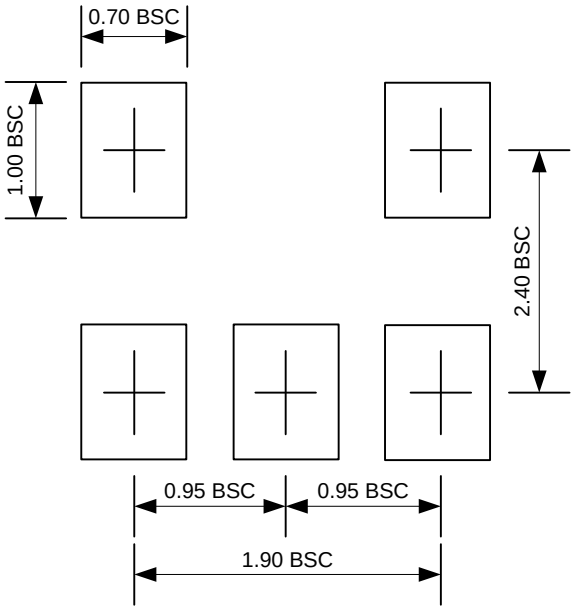
■ Package Dimension

SOT23-5



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.30	0.0354	0.0512
A_1	0.00	0.15	0.0000	0.0059
b	0.30	0.55	0.0118	0.0217
D	2.70	3.10	0.1063	0.1220
E	1.40	1.80	0.0551	0.0709
e	1.90 BSC		0.0748 BSC	
H	2.60	3.00	0.1024	0.1181
L	0.37 BSC		0.0146 BSC	
θ1	0^o	10^o	0^o	10^o
S_1	0.95 BSC		0.0374 BSC	

■ Lead Pattern

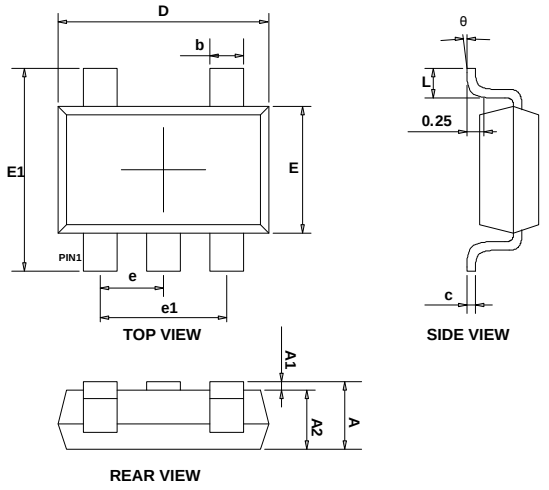


Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

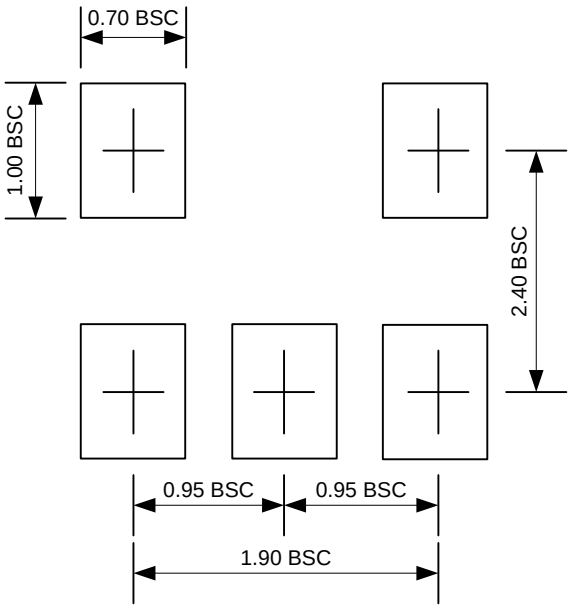
■ Package Dimension (Contd.)

TSOT23-5



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b	0.350	0.500	0.014	0.020
c	0.080	0.200	0.003	0.008
D	2.820	3.020	0.111	0.119
E	1.600	1.700	0.063	0.067
E1	2.650	2.950	0.104	0.116
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0^o	8^o	0^o	8^o

■ Lead Pattern

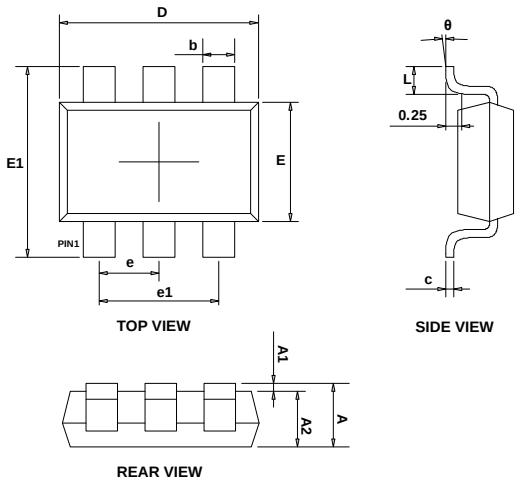


Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

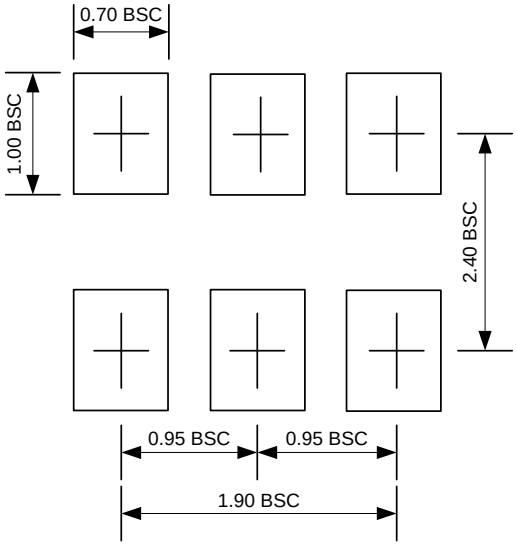
■ Package Dimension (Contd.)

TSOT23-6



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b	0.350	0.500	0.014	0.020
c	0.080	0.200	0.003	0.008
D	2.820	3.020	0.111	0.119
E	1.600	1.700	0.063	0.067
E1	2.650	2.950	0.104	0.116
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0^o	8^o	0^o	8^o

■ Lead Pattern

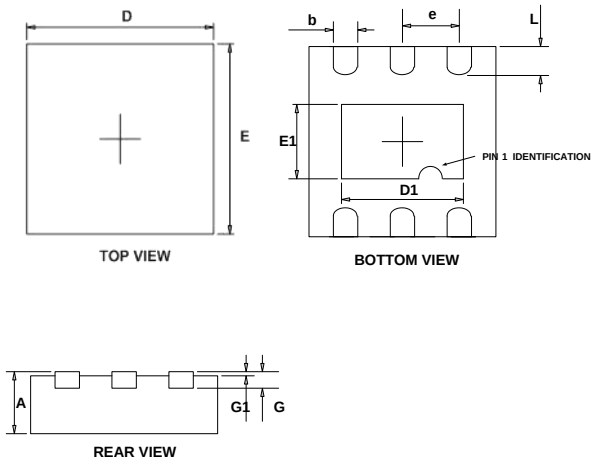


Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

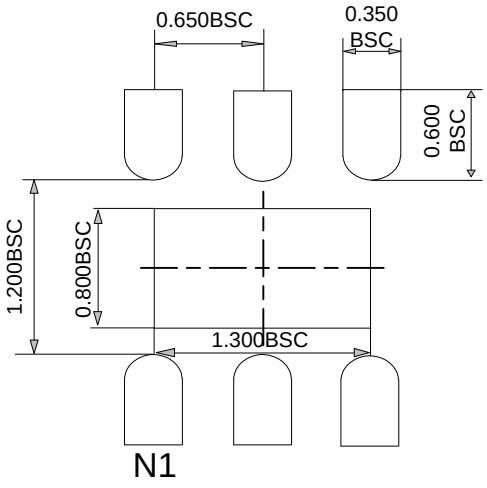
■ Package Dimension (Contd.)

DFN-6
(2x2x0.75mm)



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
e	0.650 TYP		0.026 TYP	
D1	1.100	1.650	0.043	0.065
E1	0.600	1.050	0.024	0.041
b	0.180	0.350	0.007	0.014
L	0.200	0.450	0.008	0.018
G	0.178	0.228	0.007	0.009
G1	0.000	0.050	0.000	0.002

■ Lead Pattern

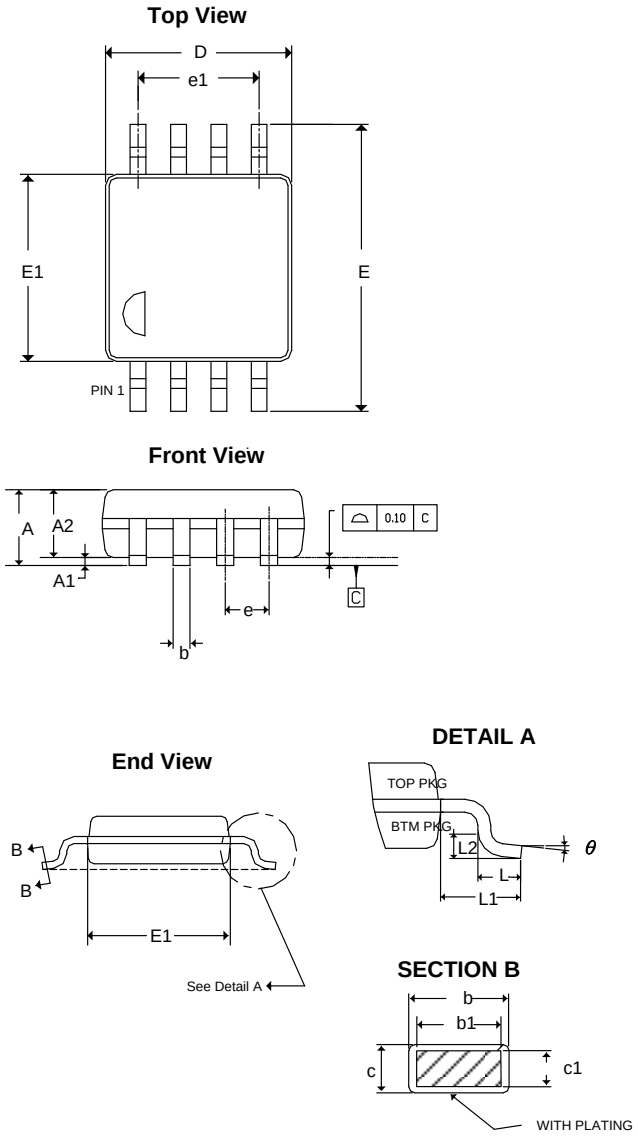


Note:

1. Dimensions in Millimeters.
2. General tolerance ±0.05mm unless otherwise specified.

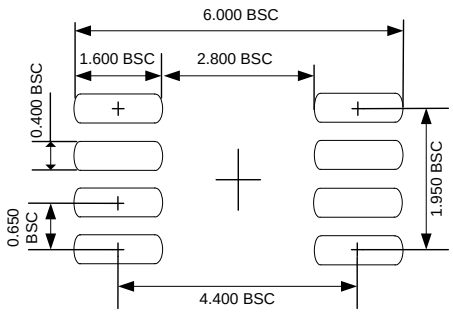
■ Package Dimension (Contd.)

MSOP-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.10	-	0.043
A_1	0.00	0.20	0.000	0.008
A2	0.75	0.95	0.029	0.037
b	0.25	0.38	0.010	0.015
b1	0.28	0.33	0.011	0.013
c	0.08	0.23	0.003	0.009
c1	0.13	0.17	0.005	0.007
D	2.90	3.10	0.114	0.122
E	4.75	5.05	0.187	0.199
E1	2.90	3.10	0.114	0.122
e	0.65 TYP		0.026 TYP	
e1	1.95 TYP		0.077 TYP	
L	0.40	0.80	0.016	0.031
L1	0.94 REF		0.037 REF	
L2	0.254 TYP		0.010 TYP	
θ	0^o	8^o	0^o	8^o

■ Lead Pattern



Note:

1. Lead pattern unit description:
   BSC: Basic. Represents theoretical exact dimension or dimension target.
2. Dimensions in Millimeters.
3. General tolerance ±0.05mm unless otherwise specified.

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